Overpack Sheet

Model 030 Cluster Controller Technical Manual

(014–002047–00)

This document contains important information about installing, programming, and operating Model 030 VMEbus–distributed (VDC/8P, VDC/16) cluster controllers. These controllers are manufactured by Systech Corporation for Data General. Accordingly, we have packaged the attached manufacturer's documentation for your use. This Overpack Sheet contains supplementary information that you will need to successfully install and operate this equipment.

NOTE: Successful operation of Model 030 cluster controllers requires downloadable software resident in DG/UX™ revision 4.32 or above. VDA/255 host adapters also depend on this software. *You cannot operate a Model 030 cluster controller or VDA/255 host adapter in systems running DG/UX™ revision 4.31 or lower.*

Getting Help from Data General

Please disregard any problem reporting procedures described in the manufacturer's documentation. For help with hardware or software problems, contact the Data General Help Line at 1–800–DG–HELPS (U.S. customers only), or contact your Data General representative at the nearest Data General office.

Warranty Information

The warranties specified in your Data General sales and field engineering contracts supersede any and all warranties referred to in the manufacturer's documentation.

WARNING: Data General Corporation does not recommend or support customer installation or maintenance of some AViiON® systems. Refer to your Data General sales and field engineering contracts for information regarding Data General warranties *before* attempting to configure, install, or remove any system components.

Installation and Maintenance

The following manuals contain basic information on configuring, installing, removing, and connecting cluster controllers in AViiON® systems.

- *HPS Downloadable Cluster Controller Installation Guide* (014–001814)
- *Setting Up and Installing VMEbus Options in AViiON® Systems* (014–001867) (for deskside systems including two VMEbus option slots)
- *Setting Up and Starting AViiON® 5000 Series Systems* (014–001806) (for office model systems including six or more VMEbus option slots)

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HPS Model 030
Cluster Controller
Technical Manual

(80-000664-4-00 Revision C)

HPS Model 030
Cluster Controller
Technical Manual

United States Patent Number 4,845,609

Change Record Page

Manual Part No. 80-000664-4-00

Date	Rev	By	Description	Pages Affected
1/5/88	A	ELB	Initial release.	All
2/9/89	erratum	ELB	Added Canadian DOC notice; added parallel printer signal information (chapter 2).	iii, vi, 1-10, 2-3, 2-4, 2-5
7/25/89	B	ELB	Incorporated 2/9/89 erratum; added HPS-7088-030 information; revised regulatory agency information.	iii – vi, 1-1, 1-3 – 1-14, 2-1 – 2-6, 3-2, 3-19, 4-3 – 4-20, D-1 – D-5
10/5/89	erratum	ELB	Added note about using proper power cord for the AC voltage applied; corrected the product weights listed in table 1-2; removed erroneous model number from appendix A.	1-13, A-4
6/6/90	C	ELB	Incorporated 10/5/89 erratum; clarified section 1.5.2 and the power requirements (table 1-2); revised the warranty and repair information.	v, 1-11, 1-13, 5-1 – 5-4, A-4

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Chapter 1
Introduction

This manual describes in detail the operation of SYSTECH Corporation's High-Performance Serial (HPS) Model 030 Downloadable Software Cluster Controllers. These models allow you to download code directly to the cluster controllers. Models covered in this manual are the HPS-7080-030, HPS-7082-030, and HPS-7088-030.

Throughout this manual, wherever the complete product name is not used, general product names of "HPS cluster controller" or "cluster controller" are used synonymously to refer to these products.

1.1 GENERAL PRODUCT DESCRIPTION

The HPS cluster controller (figure 1-1) is part of a distributed communications subsystem developed by SYSTECH for handling terminals, printers, and similar devices. This high-performance desk- or wall-mounted cluster controller is fully compatible with SYSTECH's HPS host adapters.

HPS cluster controllers provide a method of connecting clusters of eight or sixteen terminals (depending on the cluster controller model used) to a single HPS host adapter board by means of a single RG-62A/U coaxial cable. And because each cluster controller can be assigned an exclusive address (by setting externally accessed address switches), as many as fifteen cluster controllers can be "daisy chained" to the host adapter. And depending on how many cluster controllers are connected to the host adapter, the last cluster controller in the daisy chain can be located up to 1000 feet from the host adapter board (refer to section 1.3.1. for specifications regarding the coaxial line). This configuration is illustrated in figure 1-2.

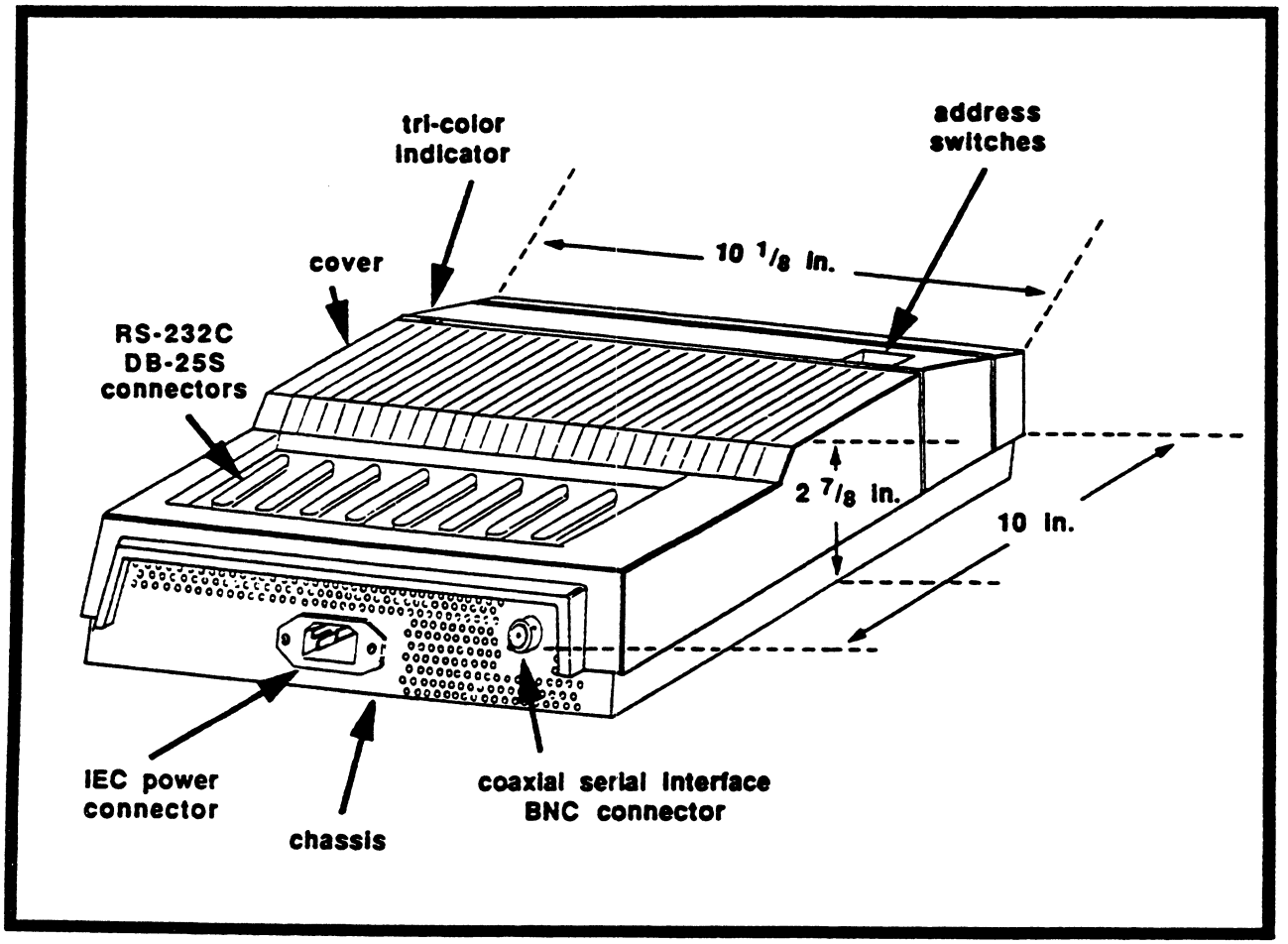

Figure 1-1. HPS Cluster Controller, Model 7080-030

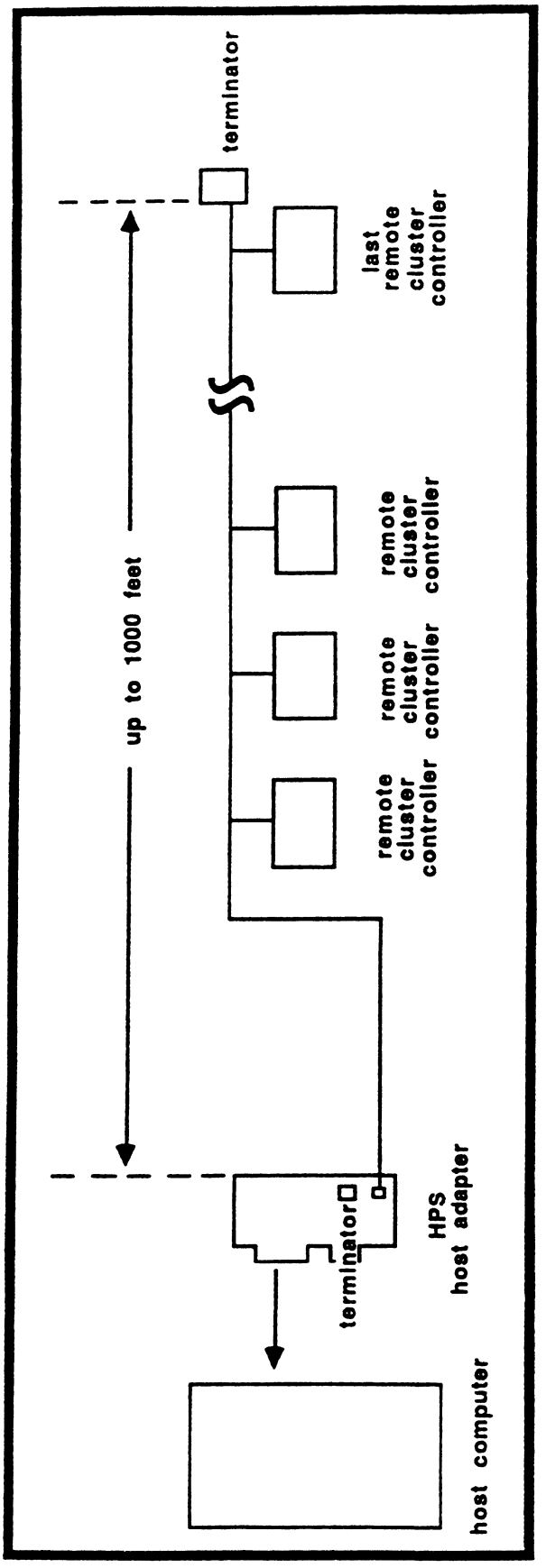

Figure 1-2. Interconnection Diagram

The coaxial cable connects to each cluster controller via a BNC "T" fitting; the signal passes through the "T" fitting on its way to the termination point. The cluster controller is transformer coupled to the cable. This ensures that a failing cluster controller, or one that is accidentally disconnected from power, will not bring the entire system to a halt. The use of a "T" fitting for interconnecting the coaxial cable and the cluster controller allows a cluster controller to be physically disconnected from the "T" fitting while the system is on-line, without breaking the coaxial connection to other cluster controllers. This feature allows you to replace or add cluster controllers (as long as a "T" fitting already exists at the location you plan to add a controller) without disturbing other users of the system.

Depending on the model used, the cluster controller provides either eight or sixteen lines of RS-232C data communication equipment (DCE) data ports via DB-25S connectors. You may program the ports individually for communication at baud rates of from 45.5 bps to 38.4K bps.

The HPS cluster controller operates on AC power delivered by a detachable power cord. The power cord plugs into an International Electrotechnical Commission (IEC) connector on the cluster controller's connector panel. A tri-color indicator light provides information regarding the operating status of the cluster controller. **SYSTECH**'s HPS Diagnostic Test Module, model 3320, can be connected to the cluster controller for extensive diagnostic testing.

Additional features of the downloadable cluster controller are:

- 10 MHz 68000 microprocessor
- 64K bytes of EPROM containing diagnostics and resident default cluster controller firmware
- 128K bytes of static RAM in downloadable cluster controllers
- 2K bytes of static RAM for coaxial serial interface buffer support
- One octal asynchronous receiver/transmitter (OctART) on the HPS-7080-030 and HPS-7082-030; two OctARTs on the HPS-7088-030

- Eight RS-232C DCE ports on the HPS-7080-030 and HPS-7082-030; sixteen channels on the HPS-7088-030
- Universal input power supply requires no changes between 115 VAC and 220 VAC
- Attractive injection-molded plastic case
- Optional wall mounting package

1.2 CLUSTER CONTROLLER MODELS

Model 030 cluster controllers handle the character-by-character processing for eight or sixteen user terminals. All models contain a 68000 microprocessor, 64K bytes of EPROM, and 128K bytes of RAM, plus the transport interface for connection to the host via daisy-chained coaxial connections. The cluster controller product line provides a number of cost/performance combinations covering a wide spectrum of configuration sizes.

The cluster controllers are packaged in an injection-molded, impact-resistant plastic case suitable for wall-mount or desktop use. Depending on the model, they provide eight or sixteen standard DB-25 connectors for the RS-232 ports. HPS cluster controllers meet UL, FCC, Canadian DOC, CSA, VDE, and TUV specifications for use in office environments as electronic data processing equipment.

The **HPS-7080-030** supports eight RS-232 asynchronous devices. The maximum data rate per port is 38.4K bps. The data rate, character length, stop bits, parity, and flow control (XON/XOFF) of each line can be programmed from the host on an individual basis.

The **HPS-7082-030** has all the capabilities of the HPS-7080-030, plus it includes a Centronics[1]-type parallel printer port. This printer port connector is installed at the "option" connector location.

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1 Centronics is a trademark of Data Computer Corporation.

The **HPS-7088-030** supports sixteen RS-232 asynchronous devices. The maximum data rate per port is 38.4K bps. This cluster controller is essentially an HPS-7080-030 with a second "slave" OctART sharing the 68000 microprocessor. It provides the same function as two eight-port cluster controllers, but does so at a lower cost and lower throughput because one CPU drives twice as many ports. This model appears as two model 7080-030 units on a double-wide chassis.

The downloadable software cluster controllers allow you to download operation code directly to the cluster controllers. This facilitates updating the code when new software releases are available. Instead of a hardware change to physically swap EPROMs containing new code with those containing the old code, the new code can simply be downloaded to the cluster controller. Note that Terminal Control Software for Downloadable Cluster Controllers (TCSD) version 03A or later is required to support the downloadable feature of the cluster controllers.

If the downloadable function is not supported by the host computer, the cluster controllers will default to PROM-based firmware for full operation.

1.3 FUNCTIONAL DESCRIPTION

1.3.1 COAXIAL SERIAL INTERFACE

HPS host adapters are connected to the cluster controllers by a flexible cabling scheme which uses RG-62A/U coaxial cable (this cable is readily available from either cable distributors or from **SYSTECH**). Up to fifteen cluster controllers can be connected to the host adapter and, depending on the number of cluster controllers connected, the last cluster controller can be located up to 1000 feet from the host.

Signal strength of a network decreases as a function of the number of nodes[2] connected and the length of the coaxial cable used. Consequently, to maintain adequate signal margins for proper operation of the product, there is a tradeoff between the maximum number of cluster controllers (nodes) that can be attached to the network and the maximum length of the coaxial network. Table 1-1 specifies the relationship between coaxial cable length and the number of nodes supported. Cable length/number of node combinations that exceed these specifications can result in excessive data transmission errors.

The line discipline on the cable is based on token-passing network technology which operates at a 2.5 Mbit/second signaling rate. The cluster controllers contain chip sets that implement the token-passing bit serial bus system in straight bus topology from the HPS host adapter which is installed in the host computer.

The user selects an exclusive address for each cluster controller. **Each HPS host adapter and cluster controller on the same network must be set to a unique, nonconflicting node address from 01 hexadecimal to FF hexadecimal. SYSTECH** recommends that the HPS host adapter address be configured as FF hexadecimal (255) and that the cluster controllers start at address 1 and increase sequentially to 0FH (15). Data on this coaxial serial data bus is controlled by the transmit enable token-passing method. When the system comes online, or if the system receives a reconfigure command, each station (host adapter and cluster controllers) searches for the next sequential responding address on the bus, starting with the station which has the highest address. The next sequential responding address becomes the token-passing destination for that particular station.

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2 A node is defined as any active device (host adapter or cluster controller) connected to the coaxial line. For example, a system configuration consisting of nine cluster controllers and one host adapter is considered to be ten nodes. Based on this example, table 1-1 shows that the maximum coaxial cable length for ten nodes is 700 feet.

Table 1-1. HPS Configuration Specifications

Number of Nodes	Maximum Cable Length
8	1000
9	800
10	700
11	650
12	600
13	550
14	500
15	400
16	350

When a station receives the token and is requested to transmit data from one of its buffers to another station (host adapter to cluster controller or cluster controller to host adapter), it sends an inquiry to the destination to verify that a data buffer is available. If the destination does not have a buffer free, it returns a "not acknowledge" to the source, which in turn passes the token to the next sequential address. If a data buffer is available, the destination returns an "acknowledge." The station holding the token then transmits the data to the destination and waits for an acknowledge. When the destination returns an acknowledge response, the transmitting station passes the token to the next sequential address on the bus. If a station receives the token, but has no need to transmit, it passes the token to the next sequential responding address on the bus. Communication on the bus continues in this fashion at a 2.5 Mbit/second rate.

1.3.2 COAXIAL SERIAL DATA TO RS-232C DCE DATA INTERFACE

The data received at each HPS cluster controller must be routed to a particular terminal, or a particular terminal must be routed out of the cluster controller with a data message. The cluster controller's microprocessor provides traffic control within the unit. As host data is received into the cluster controller, the controller's coaxial serial data interface sends an interrupt to the microprocessor as notification that it requires servicing. The microprocessor then "takes" the information from the coaxial serial data interface, decodes its destination, and routes the data to the desired terminal. If a particular terminal has data for the coaxial serial data interface, it sends an interrupt to the microprocessor as notification that it requires servicing. The microprocessor then selects the particular terminal, "takes" the data, and routes it to the coaxial serial data interface.

1.3.3 RS-232C DCE DATA INTERFACE

The HPS-7080-030 and HPS-7082-030 cluster controllers are equipped with one eight-channel OctART which controls the eight data ports; the HPS-7088-030 contains two OctARTs, providing sixteen port control. The OctART obtains and sends data to and from the RS-232C receiver/driver interface. The RS-232C signals supported are: CTS, DCD, DSR, DTR, RTS, RXD, TXD, and Ground.

1.3.4 PARALLEL PRINTER PORT INTERFACE

The parallel printer interface on the HPS-7082-030 cluster controller provides a means of connecting a parallel printer to the cluster controller. It provides the necessary drivers, receivers, and strobes to support a Centronics-type printer. The signals supported are: *DATA BITS 1* through *8*, *DATA STROBE/*, *FAULT/*, *SLCT* (select), *PE* (paper empty), and *ACKNLG/* (data acknowledge).

1.4 DIAGNOSTICS

The HPS cluster controller has an extensive self-test program which is executed upon power up or timeout/reset. The tri-color light-emitting diode (LED) indicates various status conditions during the self-test. Refer to chapter 4 for details on the cluster controller self-test.

1.5 REGULATORY AGENCY INFORMATION

1.5.1 SAFETY REGULATIONS

Model 030 cluster controllers have obtained the following safety agency approvals:

- Underwriter's Laboratories Information Processing and Business Equipment Standard UL 478, Fifth Edition.
- Canadian Standards Association (CSA) C22.2 number 220-M1986.
- TÜV International Electrotechnical Commission (IEC) 380.

1.5.2 EMISSIONS REGULATIONS

Model 030 cluster controllers have obtained VDE 0871 emissions agency approval. In addition, the cluster controllers comply with the following regulations:

- United States Federal Communications Commission (FCC) Part 15, Subpart J, Class A.
- Canadian Department of Communications (DOC) (FCC standards apply).

FCC WARNING

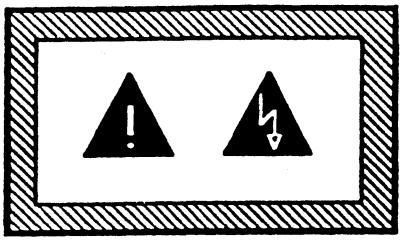
This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested with shielded I/O cabling, and nickel-plated metal shell connectors, and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Only peripherals (computer input/output devices, i.e., terminals, printers, etc.) that comply with either Class A or B FCC limits may be attached to this unit. Operation with noncompliant cables or peripherals is likely to result in interference to radio and television reception.

DOC Notice

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus as set out in the radio interference regulations of the Canadian Department of Communications.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de Classe A prescrites dans le règlement sur le brouillage radioélectrique édicté par le Ministère des Communications du Canada.



1.6 SERVICE PRECAUTIONS

Refer all servicing to qualified service personnel.

CAUTION

Electrical shock hazards inside. Do not remove cover. No user-serviceable parts inside.

VORSICHT

Um elektrischen schlag zu ver meiden mettallplatte nicht abnehmen. Zugang zur bedienung nicht erforderlich. Wartung nur durch qualifiziertes personal.

PRECAUCION

Esta cubierta no debe abrirse. Solo personal de servicio calificado. No hay partes que puedan recibir mantenimiento por el usuario.

ATTENTION

Ne pas enlever ce couvercle. Réservé au personnel autorisé. Il n´y a pas de composant à l´interieur qui puisse être remplacé par l´utilisateur.

ATTENZIONE

Non rimuovere questo coperchio. Scopritura: Solo per personale addestrato e autorizato Nell´interno non vi sono componenti che possono essere sottoposti a servzio dall´utente o fuori fabbrica.

1.7 SPECIFICATIONS

Table 1-2 lists the specifications for model 030 downloadable cluster controllers.

NOTE

Model 030 cluster controllers are equipped with auto-ranging input circuitry suitable for 120 VAC and 220 VAC operation. No adjustments are necessary. Be sure to use the proper power cord for the AC voltage applied.

Table 1-2. HPS Cluster Controller Specifications

Parameter	Specification
Dimensions	**HPS-7080-030** and **HPS-7082-030**: 2-7/8 in. high by 10-1/8 in. wide by 10 in. deep (7.3 cm high by 25.7 cm wide by 25.4 cm deep) **HPS-7088-030**: 2-7/8 in. high by 20-5/8 in. wide by 10 in. deep (7.3 cm high by 52.4 cm wide by 25.4 cm deep)
Weight	**HPS-7080-030**: 3.57 lb (1.62 kg) **HPS-7082-030**: 3.68 lb (1.67 kg) **HPS-7088-030**: 6.59 lb (2.99 kg)
Power requirements	120V/240V (92 – 249 VAC, 0.5A – 0.4A, 47 – 63 Hz)

Table 1-2. HPS Cluster Controller Specifications (Continued)

Parameter	Specification
Serial I/O interface	RS-232C
Signals supported	TXD, RXD, RTS, CTS, DTR, DSR, DCD, and Ground
Transport protocol	Token-passing bit serial bus system
Transport interface	2.5 Mbit high-impedance transceiver
Transport medium	RG-62A/U, 93 ohm coaxial cable terminated at each end with 93 ohm passive terminators
Maximum transport length	1000 foot maximum network length, without the use of HPS SYSTECH Pluriaxial Unplug Repeater (SPUR) units
Indicators	Tri-color status light-emitting diode (LED)

Chapter 2
Configuration

This chapter explains how to configure the HPS cluster controller. Installation procedures are not provided; for information on how to install the cluster controller(s) in your facility, refer to the *HPS Downloadable Cluster Controller Installation Guide.*

All configuration jumpers are preset by **SYSTECH** when manufactured and, with the exception of TO-RST, should not be changed.

2.1 JUMPER CONFIGURATION

2.1.1 TO-RST JUMPER

The timeout/reset (TO-RST) function allows the cluster controller to completely reset and reinitialize if the real-time clock advances a predetermined amount of time without having its interrupt serviced. This allows the cluster controller a method of escape if for some reason the microprocessor is instructed to service a nonexistent device or memory location. The TO-RST jumper may be installed either when developing software or when the unit is serviced and the reset is not desired. The TO-RST jumper is in the same location on all model 030 cluster controllers, however, it is numbered differently on the sixteen-channel model. Figure 2-1 identifies the TO-RST jumper as **E2** on the HPS-7080-030 and HPS-7082-030 cluster controllers, while figure 2-2 identifies it as jumper **E8** on HPS-7088-030 cluster controllers.

NOTE

When the jumper is installed, reset (watchdog timeout) cannot occur; when the jumper is not installed, resets can occur. Be sure to remove this jumper before using the cluster controller in a operating environment.

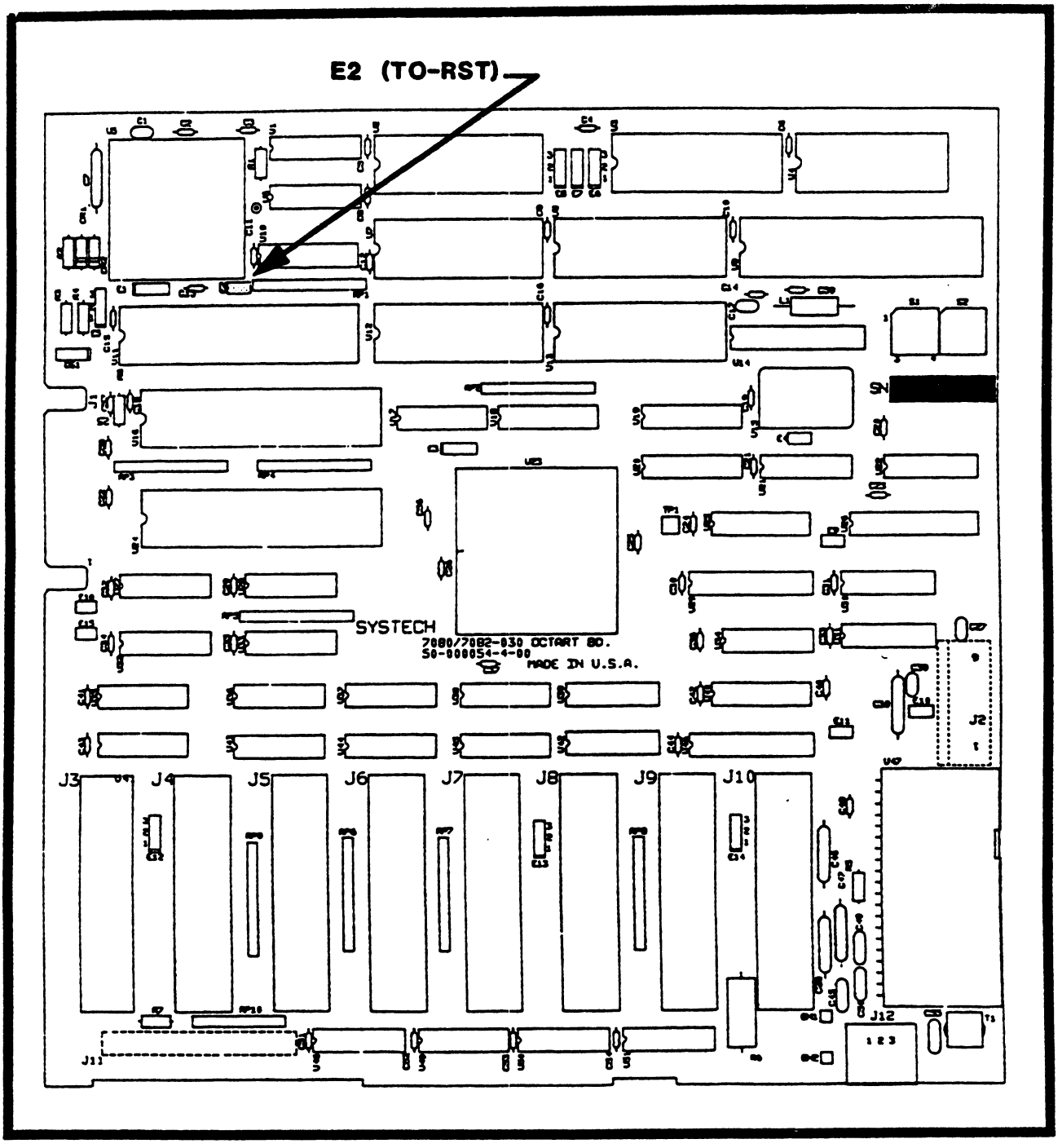


Figure 2-1. TO-RST Jumper on HPS-7080-030 and HPS-7082-030 Cluster Controllers

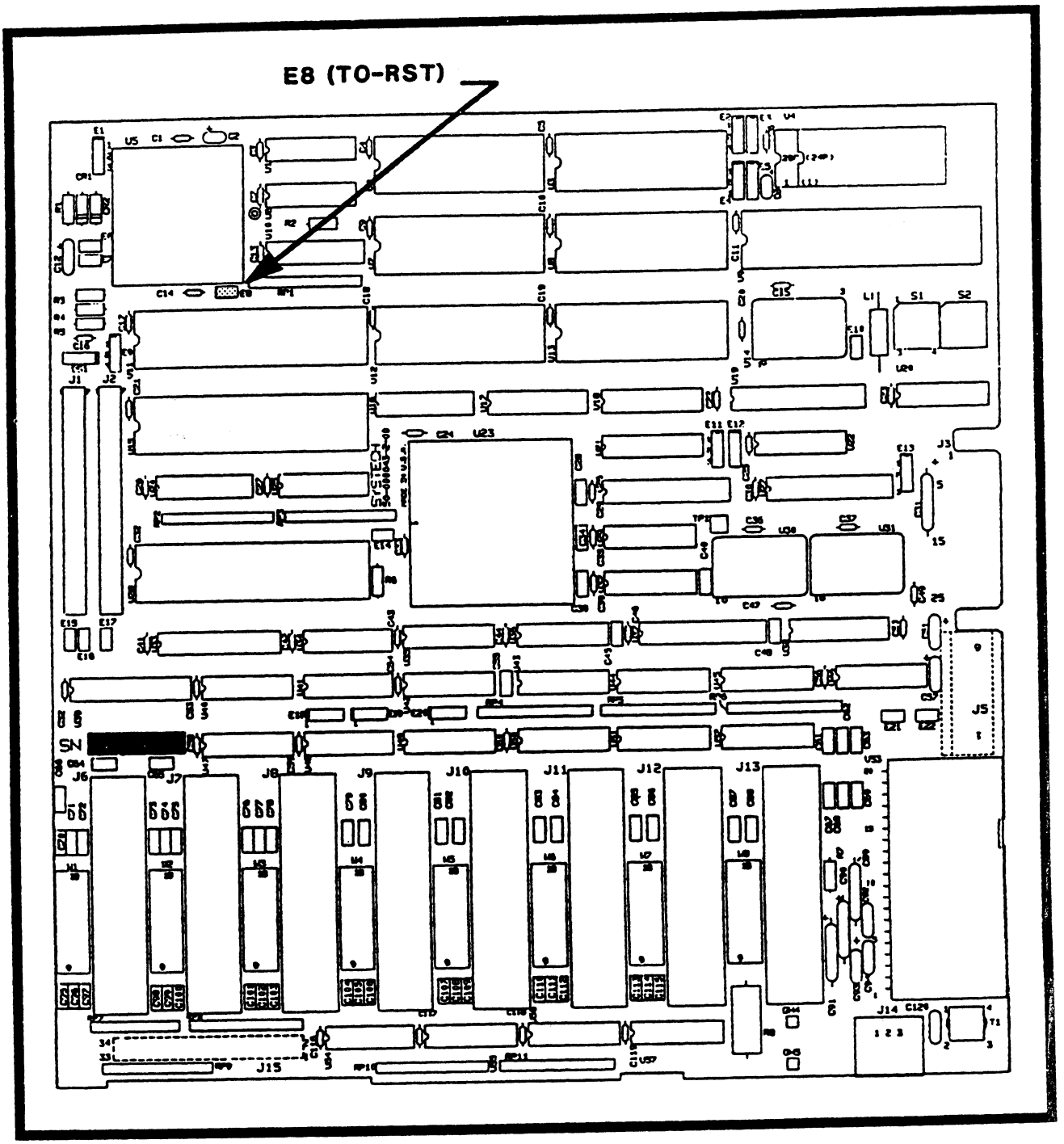


Figure 2-2. TO-RST Jumper on HPS-7088-030 Cluster Controllers

2.1.2 EPROM AND RAM JUMPERS

There are no customer-selectable EPROM or RAM jumpers.

2.2 RS-232C SERIAL INTERFACE CONFIGURATION

The serial interface on all serial ports is configured for EIA RS-232C (DCE) standards. The RS-232C receiver/driver integrated circuits are 75189/1489 and 75188/1488, respectively. Table 2-3 shows the relationship between the signals and DB-25S connector pin numbers for port connectors 0 through 7 (and 8 through 15 on sixteen-channel cluster controllers). For reference, the column labeled "Unplug™ Internal Signal Names" lists internal signal names used on cluster controller schematic diagrams. You should ignore these names unless you are referring to cluster controller schematics. The third column gives standard RS-232C signal names. As a convenient reference, the direction of each signal is also shown. The "<" symbol indicates that the signal is being received by the HPS cluster controller, and the ">" symbol indicates that the signal is being transmitted from the cluster controller.

Table 2-1. Signal/Port Connector Pin Cross Reference

DB-25S Pin Number	Unplug™ Internal Signal Name	RS-232C Signal Name
1	Protective (chassis) ground	Protective (chassis) ground
2	RXD <	TXD <
3	TXD >	RXD >
4	CTS <	RTS <
5	RTS >	CTS >
6	DTR >	DSR >
7	Signal ground	Signal ground
8	DCD* <	DCD >
20	DSR <	DTR <

* The DCD signal is pulled high (+12V) through a 5.6 kΩ resistor.

2.3 PARALLEL PRINTER INTERFACE SIGNALS

The HPS-7082-030 cluster controller supports a Centronics-type parallel printer port. The drivers on all output signals to the parallel printer are of the open collector type (i.e., 7416, 7417). These driver outputs are terminated to +5V by a 1K ohm resistor.

All input signals to the parallel printer are low-impedance terminated by a 220 ohm resistor to +5V, and a 330 ohm resistor to ground. Table 2-2 lists the signals supported by the parallel interface port.

Table 2-2. Parallel Printer Signals Supported

Printer I/O Connector Pin	Signal Name	Direction In/Out	Sink Current (If Output)	Termination
1	DATA STROBE/	output	35 mA	1K ohm to +5V
2	DATA 1	output	35 mA	1K ohm to +5V
3	DATA 2	output	35 mA	1K ohm to +5V
4	DATA 3	output	35 mA	1K ohm to +5V
5	DATA 4	output	35 mA	1K ohm to +5V
6	DATA 5	output	35 mA	1K ohm to +5V
7	DATA 6	output	35 mA	1K ohm to +5V
8	DATA 7	output	35 mA	1K ohm to +5V
9	DATA 8	output	35 mA	1K ohm to +5V
10	DATA ACK/	input	N/A	220 ohm to +5V 330 ohm to GND
12	PAPER EMPTY	input	N/A	220 ohm to +5V 330 ohm to GND
13	SELECT	input	N/A	220 ohm to +5V 330 ohm to GND

Table 2-2. Parallel Printer Signals Supported (Continued)

Printer I/O Connector Pin	Signal Name	Direction In/Out	Sink Current (If Output)	Termination
19	COMMON (DS/)	N/A	N/A	N/A
20	COMMON (D1)	N/A	N/A	N/A
21	COMMON (D2)	N/A	N/A	N/A
22	COMMON (D3)	N/A	N/A	N/A
23	COMMON (D4)	N/A	N/A	N/A
24	COMMON (D5)	N/A	N/A	N/A
25	COMMON (D6)	N/A	N/A	N/A
26	COMMON (D7)	N/A	N/A	N/A
27	COMMON (D8)	N/A	N/A	N/A
28	COMMON (DAK)	N/A	N/A	N/A
29	COMMON	N/A	N/A	N/A
32	FAULT/	input	N/A	220 ohm to +5V 330 ohm to GND
33	COMMON	N/A	N/A	N/A

Chapter 3
Theory of Operation

This chapter describes the internal operation of the HPS cluster controller. A detailed description of hardware operation follows a brief overview of the major hardware components.

3.1 HARDWARE OVERVIEW

Refer to the block diagram in figure 3-1 as you read the following sections.

NOTE

Complementary metal-oxide semiconductor (CMOS) components are used in the HPS cluster controller. Because these CMOS components are sensitive to electronic discharge, observe proper static control procedures when handling the printed circuit board.

3.1.1 THE CPU

The HPS cluster controller was designed around a 10 MHz 68000 microprocessor.

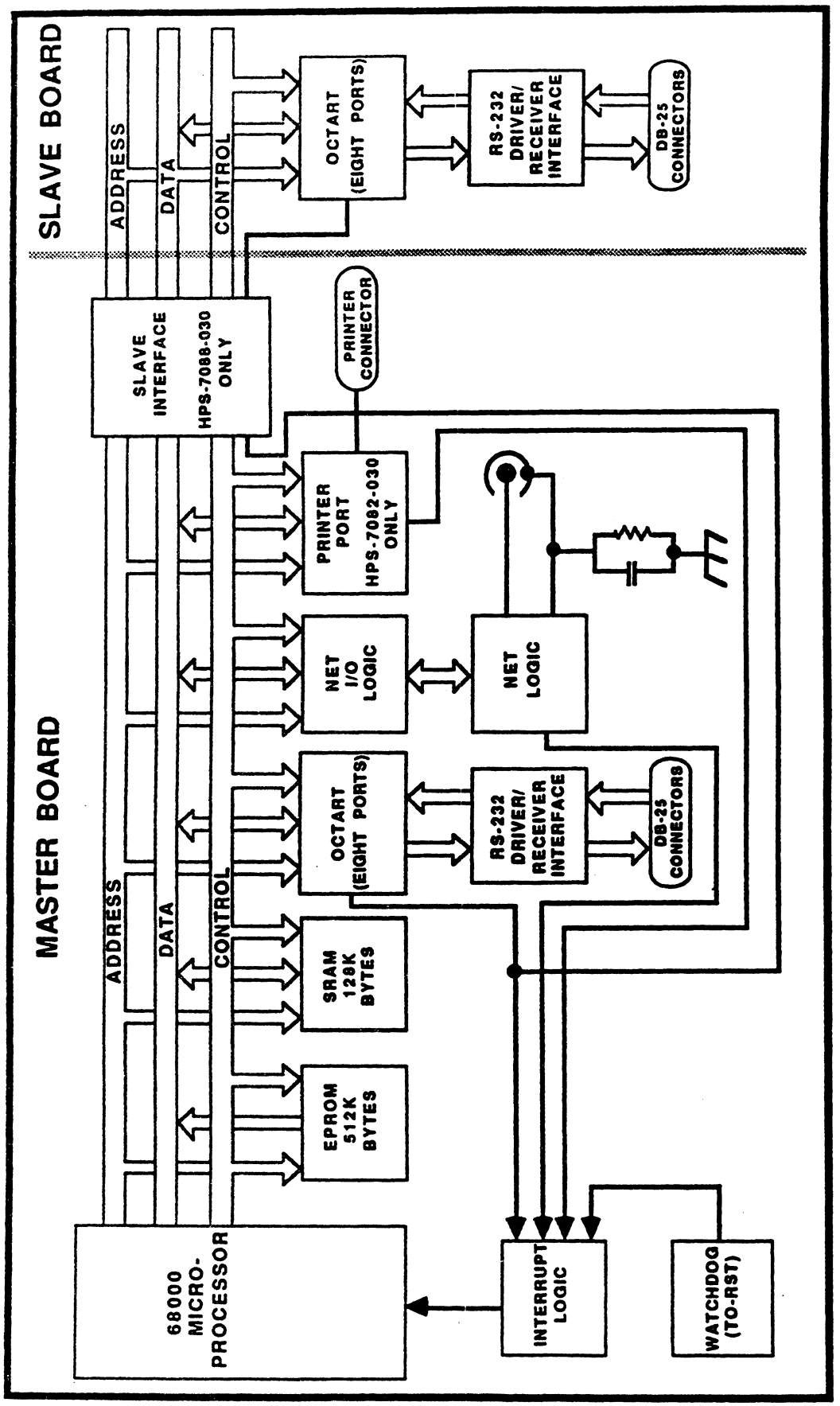


Figure 3-1. Functional Block Diagram

3.1.2 EPROM

The cluster controller is equipped with two JEDEC 28-pin sockets that are configured for 27256 EPROMs. Note that 150 ns EPROMs are required in the cluster controller.

3.1.3 LOCAL STATIC RAM

The cluster controller is equipped with four JEDEC 28-pin IC positions that are configured for 32K x 8 static RAMs (SRAMs). Note that 120 ns SRAMs are required.

3.1.4 NETWORK INTERFACE

The COM 9026, REM4B, and 9058S family was chosen for its token-passing bit serial data bus interface. A 2K x 8 dual-port SRAM provides a memory-mapped data interface between the network and the CPU. The SRAM can contain up to four pages of input or output data, with each page containing up to 508 bytes of data (4 of the 512 bytes are control bytes).

3.1.5 RS-232C INTERFACE

A custom OctART, designed by SYSTECH, provides the RS-232C interfacing. This 84-pin PLCC CMOS OctART provides eight serial ports per chip. The RS-232 drivers and receivers are the 75188/1488 and 75189/1489, respectively.

3.2 DETAILED HARDWARE OPERATION

3.2.1 SYSTEM CLOCK

The system clock is a 20 MHz clock oscillator module. The system clock interfaces directly with the token-pass bit serial bus interface, and is divided in half to provide the 10 MHz CPU clock.

3.2.2 RESET CIRCUIT

A reset pulse provided at power-up clears the cluster controller and initializes the CPU supervisor stack pointer. An RC network generates this reset externally to a buffer which drives both the CPU *HALT* and *RESET* signals. The reset, in both "true" and "not true" states, is routed throughout the cluster controller to reset registers, flip-flops, and LSI devices.

3.2.3 DTACK CIRCUIT

The DTACK circuit informs the CPU that the addressed device has received/ transmitted its data and is ready to end the cycle in progress. The summation of all these device "cycle complete" signals occurs at the microprocessor on a TTL signal bus that is not "open drain."

3.2.4 INTERRUPT CIRCUIT

The HPS cluster controller responds to six levels of interrupts. The priority of the interrupt is selected by an eight-level priority encoder connected to the microprocessor. The priority levels, from maximum to minimum priority are:

- **Level 7 - Factory test use only**

- **Level 6 - OctART receive interrupt**

  If an OctART receive interrupt is detected, a level 6 interrupt is passed to the microprocessor.

- **Level 5 - Real-time clock interrupt**

  A free-running clock sets an interrupt approximately every 52 ms which is passed to the microprocessor as a level 5 interrupt. If another 52 ms passes without the level 5 interrupt being serviced, the cluster controller is declared "dead" and a real-time clock timeout reset is issued, resetting the cluster controller.

- **Level 4 - OctART transmit interrupt**

  If an OctART transmit interrupt is detected, a level 4 interrupt is passed to the microprocessor.

- **Level 3 - Network interrupt**

  When the network logic needs to be serviced, a level 3 interrupt is passed to the microprocessor.

- **Level 2 - OctART modem interrupt**

  A modem interrupt is generated and passed to the microprocessor if any OctART channel needs servicing for any reason.

- **Level 1 - Option interrupt**

  The option interrupt detects the printer port interrupt on the model 7082-030 cluster controller.

3.2.5 MICROPROCESSOR

The 10 MHz 68000 microprocessor drives 16 unbuffered data lines and 23 unbuffered address lines. The microprocessor responds to six levels of interrupts, and can transmit as well as receive a reset. When an interrupt occurs, the microprocessor "function code output" is decoded and inverted to provide the "not valid peripheral address" (*VPA/*), inhibiting a *DTACK/* response for autovector operation.

3.2.6 DEVICE BLOCK ADDRESSING

Because the CPU views all devices as memory addresses, memory and devices share the same block addressing logic. The block memory/devices are selected by a custom application-specific integrated circuit (ASIC).

3.2.7 OctART SUBADDRESSING

Once the block address for the OctART has been decoded, decoding is necessary to select the desired OctART channel, or register. Lower address bits to the OctART handle the subdecoding.

3.2.8 MEMORY MAP LOGIC

Hardware maps the lowest 1K of EPROM to the lowest 1K of RAM. This was done because the vector tables, which reside in the lowest 1K of EPROM, need specific values upon power-up; however, they require the ability to be modified during operation and no microprocessor memory-mapping instruction exists. By mapping the lowest 1K of EPROM to the lowest 1K of RAM, after power-up, power-up diagnostics, and initialization, the "memory map logic" can be enabled and then any EPROM address from 0 to 3FFH will automatically select RAM address 100000H to 1003FFH.

Writing to location 70000H to 7FFFFH ("don't care" data) enables the memory map. Either writing to location 60000H to 6FFFFH ("don't care" data), a power-up reset, or a reset clears this function.

"Memory map enable" qualifies the decoding of the map address. If an address of 400H or higher is selected, the EPROM qualified by the EPROM-select signal (*EPROMSEL/*) will be selected. If an address of 3FFH or lower is selected, RAM0, qualified by the EPROM-not-select signal (*EPROMSEL/*) will be selected.

3.2.9 EPROM

When the one-of-eight octal decoder selects the EPROM block, the *EPROMSEL/* signal is routed to memory map logic. If memory map is enabled, there is a possibility that RAM0 will be selected. This happens if the EPROM location selected is 3FFH or lower.

If memory map is enabled but the address is 400H or higher, EPROM will be selected. EPROM will be selected in all *EPROMSEL/* addresses if memory map is not enabled. For example, the *EPROMSEL/* becomes *MEPROMSEL/*, and continues to the "not chip enable" pin of the EPROM.

3.2.10 RAM

Once the RAM subaddressing is completed, and depending on the addressing, either RAM0 or RAM1 is selected. Note that there is a low byte RAM0 and RAM1 as well as a high byte RAM0 and RAM1.

To "read" a RAM, the *WT-RD/* signal on the RAM "not output enable" pin must be low and the *LOBYWT/* and *HIBYWT/* signals on the RAM "read/not write" pin must be high. To "write" a RAM, the *WT-RD/* signal on the RAM "not output enable" pin must be high, and the *LOBYWT/* and *HIBYWT/* signals on the RAM "read/not write" pin must be low. Keep in mind that because the lower 1K of RAM is reserved for memory mapping, the first actual usable RAM address is 100400H. Note that *RAMSEL/* generates an immediate *DTACK/* to allow the CPU to complete the current cycle.

3.2.11 OCTART

The cluster controller uses a custom OctART for RS-232 I/O control. When the OctART address block is selected, the OctART is "written into" or "read from" depending on the status of the *RD-WT/* signal. No other enables or strobes are needed. (For additional information on the OctART, refer to the Swallow OctART document.)

The bit rate generator clock is the same 10 MHz clock that drives the microprocessor. All bit rates supported may be selected in the OctART. The receive and transmit signals are connected to 75189/1489 RS-232 receivers and 75188/1488 RS-232 drivers. Note that the OctART provides the *DTACK/* signal on an open drain output. The model 30 cluster controllers support bit rates of 45.5, 50, 75, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, 2000, 2400, 3000, 3600, 4200, 4800, 5400, 6000, 6600, 7200, 7800, 8400, 9000, 9600, 10200, 10800, 19200, and 38400 bps.

3.2.12 TOKEN-PASS BIT SERIAL BUS LOGIC

3.2.12.1 Network Interface

The address and data lines are buffered and latched between the microprocessor and the COM 9026. The COM 9026 uses a multiplexed address and data bus from 0 through 7. Two quad two-line to one-line data selectors provide access to the COM 9026 AD0 through AD7 from the microprocessor local data and local address buses. To provide latched memory addresses to the 2K x 8 SRAM, an octal D-type latch is used. A 4-bit D-type register latches address bits 8 through 10 for the SRAM and COM 9026 addressing from the CPU. An octal D-type latch provides a data feedback route from the 2K x 8 SRAM to the CPU.

3.2.12.2 COM 9026 and Related Logic

The COM 9026 interfaces with the microprocessor via the network interface (discussed above). It also has complete control of the 2K x 8 SRAM and can store up to four "pages" of data packets as large as 512 bytes each (4 of which are network control bytes). These pages can be for information either transmitted from the CPU or received from the network.

The COM 9026 also interfaces with the address switch data. The address switch information is parallel loaded into a custom ASIC, clocked most significant bit (MSB) first, and sampled by the COM 9026. In this way the COM 9026 verifies packet addresses on the net to see if any address matches its own. The COM 9026 also interfaces to the custom ASIC REM4B (discussed below).

If the COM 9026 is selected with either a *NETI/O/* or a *NETMEM/* when it is busy, it will assert a *NETWAIT* signal to the *NETWAIT* flip-flop. The flip-flop is enabled when *NETSEL/* goes true (a negative NOR of *NETI/O/* and *NETMEM/*). When the COM 9026 is ready for data, *NETWAIT* drops, the flip-flop clocks, and *DTACK/* is asserted for CPU cycle completion. (Refer to the Standard Microsystems Corporation data sheet on the COM 9026 for specific details about this chip.)

3.2.12.3 Network Transceiver - REM4B

This single chip provides interfacing between the controller (COM 9026) and the high impedance transceiver (COM 9058S). This chip provides the COM 9026 clock (derived from the 20 MHz system clock), and either converts the serial receive data to NRZ data for the COM 9026, or converts the COM 9026 transmit data to the form needed by the COM 9058S to drive the token-pass bit serial bus interface. This device also provides the shift register for the parallel-to-serial conversion of the address switches.

3.2.12.4 HIT - COM 9058S

This hybrid module interfaces directly with the token-pass bit serial bus. Note that the outer ring of the BNC connector (shield) does not, and should not attach directly to ground. The outer ring (the coaxial shield connection) is decoupled to ground through a 0.01 µF capacitor in parallel with an 11 kilohm resistor. (Refer to the Standard Microsystems Corporation data sheet for specific details about this component.)

3.3 TYPICAL CPU CYCLES

The following sections describe the various read and write cycles performed by the CPU. Refer to figures 3-2 and 3-3 for typical read and write cycles, respectively.

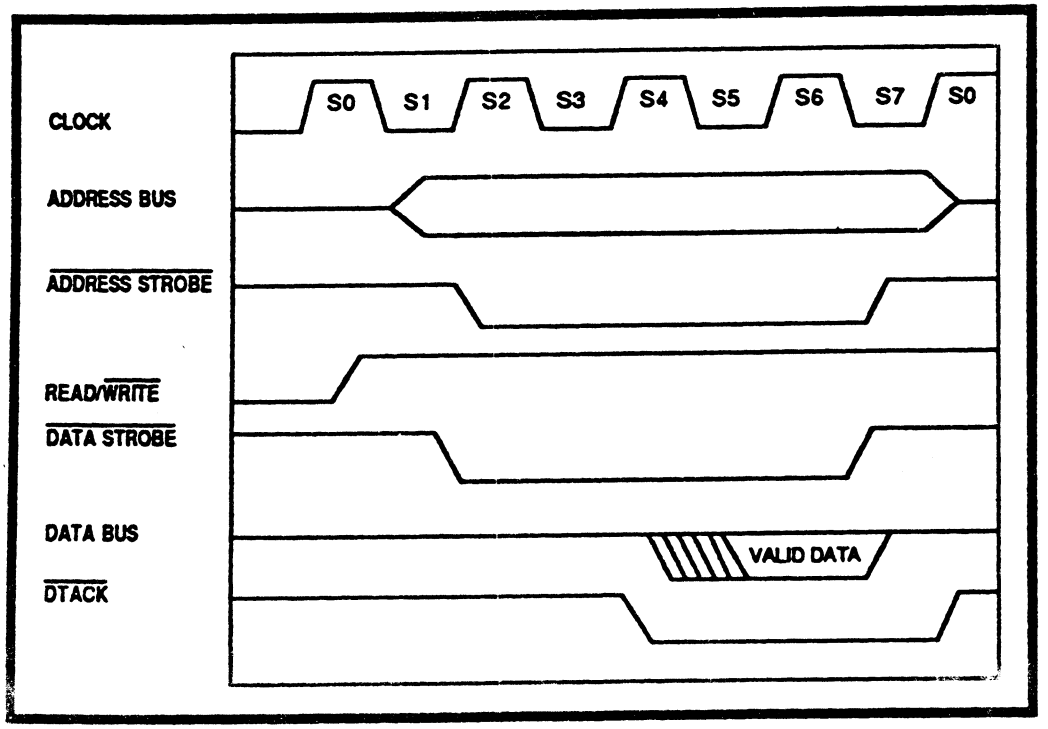


Figure 3-2. Typical EPROM/RAM Read Cycle

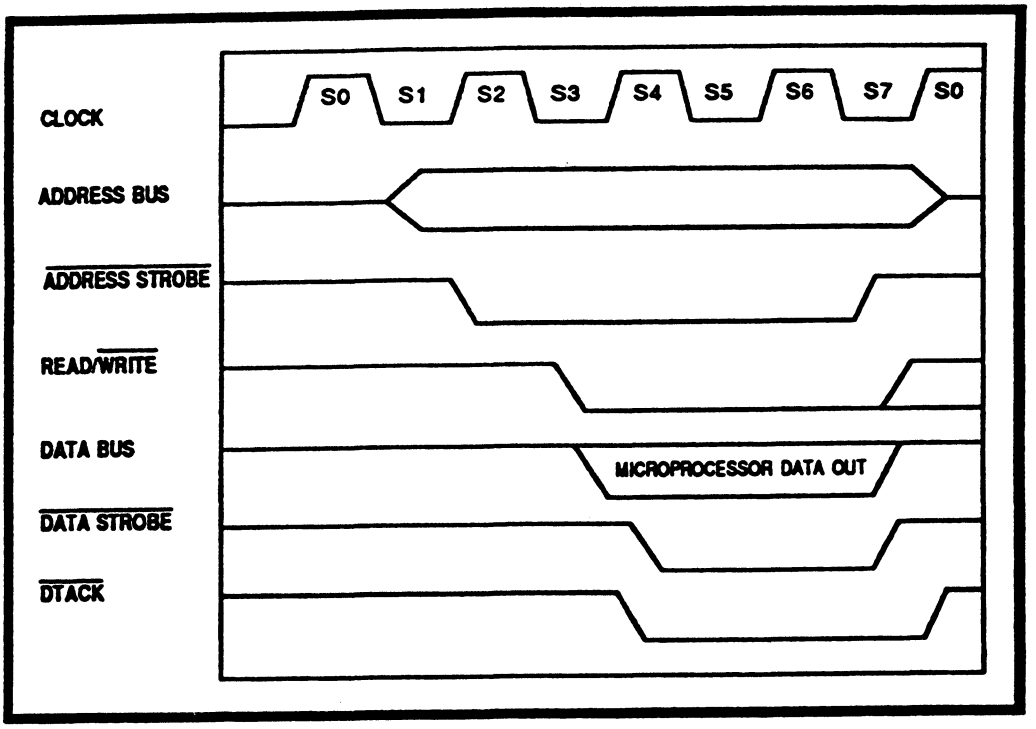


Figure 3-3. Typical RAM Write Cycle

3.3.1 EPROM READ CYCLES

At the beginning of an EPROM read cycle, the microprocessor addresses the byte of EPROM selected during microprocessor state S1. During S2, the microprocessor asserts the address strobe, indicating that a valid address exists on the address bus. At about the same time that the address strobe is asserted, the data strobe is asserted, however, this signal isn't used until the cycle is completed. A one-of-eight octal decoder handles EPROM selection. The EPROM select signal is decoded and if memory map is not enabled, EPROM is directly selected. If memory map is enabled and the address is 0H through 3FFH, we have a map-to-RAM condition and RAM0 (both low and high byte) is selected.

Whether EPROM or RAM is selected, valid data will occur on the data bus (LD0 through LD15) within 150 ns of the time selected. Near the beginning of S4, *DTACK/* is sent to the CPU from the DTACK circuit. This signals the CPU that the present bus cycle may be terminated. The CPU removes the address strobe soon after the trailing edge of S6, latching data into the microprocessor. This in turn terminates *EPROMSEL/*, which in turn terminates *RAM0ENBL/* or *MEPROMSEL/* (whichever was selected). At approximately the same time that the address strobe terminates, the data strobe terminates, latching data into the microprocessor.

3.3.2 RAM READ CYCLE

At the beginning of a RAM read cycle (during S1), the microprocessor places the desired RAM byte on the local address bus. During S2, the address strobe is asserted, indicating that a valid address is on the address bus. About the same time that the address strobe is asserted, the data strobe is asserted, indicating that the microprocessor desires valid data. The major RAM memory block is decoded by the REM1. The REM1 also provides input to the DTACK circuit to begin terminating the RAM read cycle.

Once the individual RAM pair has been decoded and the local address bus bits have decoded the individual byte, if the RD-WT/ signals (LOBYWT/ and HIBYWT/) are high within 150 ns, data will appear on local data bus LD0 through LD15. During S7, the microprocessor terminates the data strobe, latching the valid data into the the microprocessor itself. The address strobe also terminates; in turn *RAMSEL/*, the individual RAM selected, and ultimately, the RAM read cycle are also terminated.

3.3.3 RAM WRITE CYCLE

At the beginning of a RAM write cycle (during S1), the microprocessor places the desired RAM byte on the local address bus. During S2, the address strobe is asserted, indicating that a valid address is on the address bus. After the trailing edge of S2 "falls," data is asserted on the local data bus. The microprocessor asserts the data strobe 20 ns or more after data is asserted, indicating that valid data exists on the data bus. The major RAM memory block is decoded in the REM1, which also provides input to the DTACK circuit to begin terminating the RAM write cycle.

Once the individual RAM has been decoded and the local address bus bits have decoded the individual byte, if the *LOBYWT/* and *HIBYWT/* signals are low, the RAM is enabled to have data written into it. During S7, the microprocessor terminates the data strobe which terminates and latches data into the RAM. Likewise, the microprocessor terminates the address strobe, which in turn terminates the individual RAM selected and, ultimately, the RAM write cycle.

3.3.4 OCTART READ CYCLE

At the beginning of an OctART read cycle (during S1), the microprocessor places the block address of the OctART and the desired OctART subaddressing register on the local address bus. The major OctART memory block addressing is decoded by the REM1. During S2, the address strobe is asserted, indicating that a valid address is on the address bus. At about that same time that the address strobe is asserted, the data strobe is asserted, indicating that the microprocessor desires valid data. The OctART provides input to the DTACK circuit to terminate the OctART read cycle.

3.3.5 OCTART WRITE CYCLE

At the beginning of an OctART write cycle (during S1), the microprocessor places the address of the OctART and the desired OctART subaddressing register on the local address bus. The major OctART memory block addressing is decoded by the REM1. During S2, the address strobe is asserted, indicating that a valid address is on the address bus. After the trailing edge of S2 "falls," data is asserted on the local data bus (LD0 through LD15). The microprocessor asserts the data strobe 20 ns or more after the data is asserted, indicating that valid data exists on the data bus. The OctART provides input to the DTACK circuit to terminate the OctART write cycle.

3.3.6 NET I/O/NET MEM READ CYCLE

At the beginning of a NET I/O/NET MEM read cycle (during S1), the microprocessor places the desired NETI/O or NET RAM byte on the local address bus (LA1 through LA23). During S2, the address strobe is asserted, indicating that a valid address is on the address bus. About the same time that the address strobe is asserted, the data strobe is asserted, indicating that the microprocessor desires valid data. The net memory block is decoded by the REM1. *NETSEL/* enables a wait-state flip-flop to provide an input to the DTACK circuit (after *NETWAIT* goes true, or low) to begin terminating the NET I/O/NET MEM read cycle. *NET MEM/* and *NET I/O/* also enables the COM 9026 to begin a processor interface cycle.

The COM 9026 controls all CPU access to itself and to its 2K x 8 SRAM. As NETI/O or NET MEM is asserted to the COM 9026, it responds by raising its *NETWAIT* output. The CPU, seeing no *DTACK/* from the net, enters a wait state. It continues to wait until the COM 9026 drives the *NETWAIT* signal low, causing the "NET WAIT" flip-flop to declare *DTACK/*. Note that this may happen up to 1.3 µs later. *DTACK/* causes the microprocessor to begin completing the cycle. During this time, the COM 9026 places valid I/O/MEM data on LD0 through LD7. As the microprocessor cycle completes, the data strobe terminates, latching the valid data into the microprocessor. The address strobe also terminates, in turn terminating the NET I/O/NET MEM selection and ultimately, terminating the read cycle.

3.3.7 NET I/O/NET MEM WRITE CYCLE

At the beginning of a NET I/O/NET MEM write cycle (during S1), the microprocessor places the desired NETI/O or NET RAM byte on the local address bus (LA1 through LA23). During S2, the address strobe is asserted, indicating that a valid address is on the address bus. After the trailing edge of S2 "falls," data is asserted on the local data bus (LD0 through LD7). The microprocessor asserts the data strobe 20 ns or more after the data is asserted, indicating that valid data exists on the data bus. The net memory block is decoded by the REM1. *NETSEL/* enables a wait-state flip-flop to provide an input to the DTACK circuit (after *NETWAIT* goes true, or low) to begin terminating the NET I/O/NET MEM write cycle. *NET MEM/* and *NET I/O/* also enable the COM 9026.

The COM 9026 controls all CPU access to itself and to its 2K x 8 SRAM. As *NETI/O* or *NET MEM* is asserted to the COM 9026, it responds by raising its *NETWAIT* output. The CPU, seeing no *DTACK/* from the net, enters a wait state. It continues to wait until the COM 9026 drives the *NETWAIT* signal low, causing the net wait flip-flop to declare *DTACK/*. Note that this may happen up to 1.3 µs later. *DTACK/* causes the microprocessor to begin completing the cycle. During this time, the microprocessor places valid data on LD0 through LD7. The COM 9026 routes and writes the data to its destination. As the microprocessor cycle completes, the data strobe terminates; the address strobe also terminates, which in turn terminates the NET I/O/NET MEM selection and ultimately, the write cycle.

3.3.8 HPS-7082-030 INTERFACE

3.3.8.1 Printer Interface Timing Specifications

The HPS-7082-030 supports a Centronics-type printer interface. The printer data setup time is 600 ns, followed by a printer data strobe of 800 ns. The data hold after strobe is longer than 1 µs, because the data is held until the next printer data write cycle. This time is dependent on the microprocessor print data intercharacter processing, microprocessor speed, and other processing functions handled by the microprocessor between print characters. The printer interface timing diagram appears as figure 3-4.

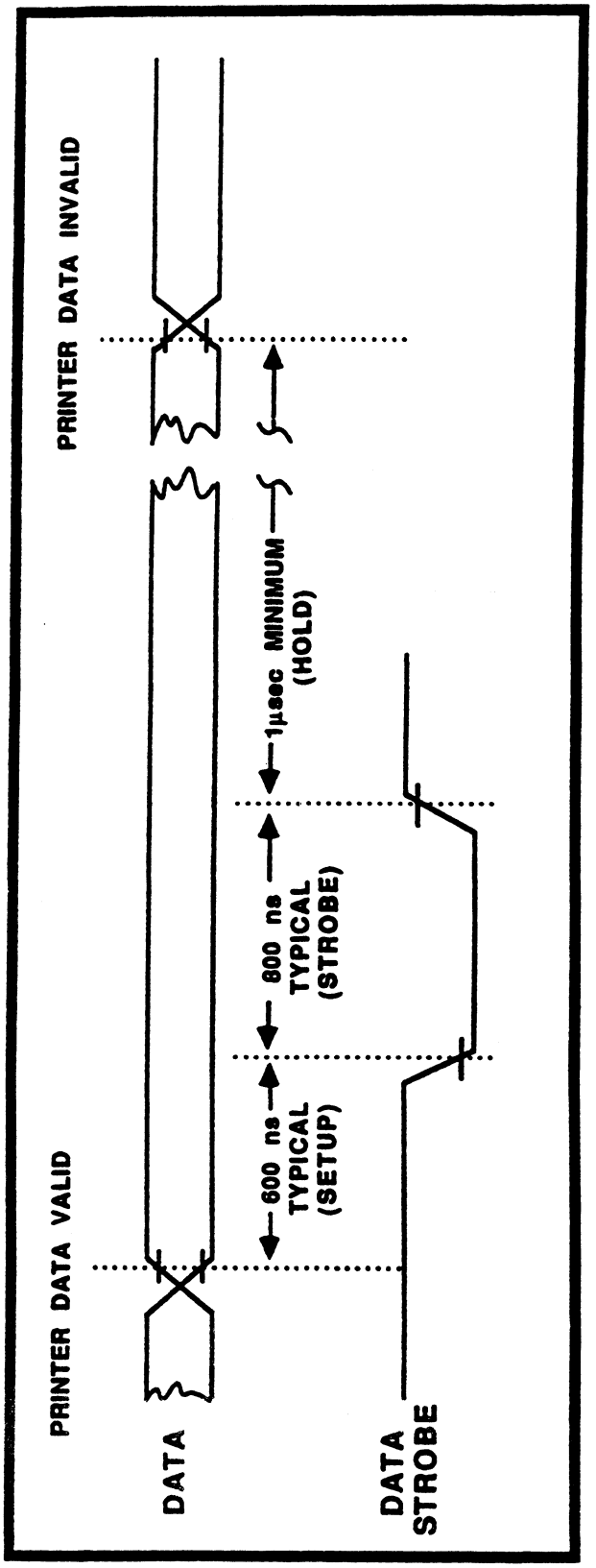


Figure 3-4. Printer Interface Timing Diagram

3.3.8.2 Printer Interface Registers

The printer interface has seven internal registers, as listed in table 3-1 and described below.

- **Printer data register**

  The printer data register is used for writing data to the printer. If a sample of what was written to the printer is desired, the printer data register can be read. Reading the printer data register will not create a data strobe to the printer.

- **Configuration register**

  The configuration register is used for programming the operating configuration of the printer port. If verification of the configuration is desired, the configuration register can be read.

- **Interrupt register**

  The interrupt register is a monitor of all items in the printer/printer interface which may need attention. There is no access for writing to the interrupt register, so the only way to clear an interrupt is to either mask it in the configuration register or service the interrupt.

- **Loopback Configuration Register**

  The loopback configuration register provides a means to loopback test the logic within the printer I/O option.

Table 3-1. Printer Interface Registers

Address	Write Function	Read Function
D0000H	Write printer data register	Read printer data register
D0002H	Write configuration register	Read configuration register
D0004H	no write function	Read interrupt register
D0006H	Write loopback configuration register	Read loopback configuration register

3.3.8.3 Data Write Cycle

The actual printer data is written one byte at a time. After a byte of data has been written to the data register, the microprocessor returns to perform other functions while waiting for a printer interrupt (microprocessor level 1 "option interrupt"). When the data is written to the data register, a delay strobe begins which will trigger the printer *DATA STROBE/*. The completion of the *DATA STROBE/* clocks the data into the printer. No further action takes place until the printer responds with an *ACKNLG*. The data acknowledge sets an *ACKNLG* flip-flop, and if the *ACKNLG* interrupt enable bit in the command register is set, an "option interrupt" occurs, completing the data write cycle.

3.4 HPS-7088-030 INTERFACE

3.4.1 SLAVE INTERFACE AND BUFFER

The HPS-7088-030 consists of a master and a slave board. The master board buffers address and data busses for expansion to the slave board. Necessary control signals and the buffered address and data busses are connected to the slave board via a pair of multi-conductor ribbon cables.

3.4.2 SLAVE LOGIC

The slave logic functions similarly to that of the master board in the areas defined below:

- **RS-232C Interface:** The RS-232C interface logic is identical to that described in section 3.1.5.
- **Interrupt Circuit:** The interrupt circuit logic responds only to interrupt levels 6, 4, and 2 described in section 3.2.4.
- **Read and Write Cycles:** EPROM read and RAM write cycles are handled as described in sections 3.3.1 and 3.3.3, respectively.

Chapter 4
Self-Test Operation

The HPS cluster controller performs a series of self-tests each time it is powered up.

These tests thoroughly check the HPS cluster controller hardware, in addition to performing a ROM checksum to ensure firmware integrity. The self-tests normally run without user intervention, however, with the aid of an HPS Diagnostic Test Module (DTM), model 3320, the self-test procedure can be monitored by the codes displayed on the DTM's two hexadecimal display light emitting diodes (LEDs).

4.1 LED OPERATION

During self-test, the cluster controller's LED flashes yellow at a rate of approximately 10 Hz. It will not change color or rate until one of three conditions exists:

- Self-test completes with no faults detected
- A failed port (either serial or parallel) is detected
- The self-test fails and either an attached DTM is set to 02 or the cluster controller's TO-RST jumper is installed.

The color/rate variations that may be exhibited by the LED are described in sections 4.1.1, 4.1.2, 4.1.3, and 4.1.4.

4.1.1 GREEN HEARTBEAT

When self-test completes without any faults being detected, the LED starts blinking in what is referred to as the green "heartbeat" pattern. The LED blinks green twice in quick succession, and then pauses before blinking twice again. This indicates that the cluster controller is waiting to be downloaded. The LED turns solid green when the download is complete and control is either transferred to the downloaded code or to the internal ROM Terminal Control Software. Refer to the *HPS Cluster Controller Download Package User Manual* for more information about downloading the cluster controller.

4.1.2 RED/GREEN HEARTBEAT

When one or more--but not all--of the ports (either serial or parallel) are found to be defective, the LED starts blinking in a red/green heartbeat pattern. The LED blinks red and then green in quick succession, and then pauses before repeating the pattern. This indicates that the cluster controller is waiting to be downloaded, but that not all of the ports are functional.

NOTE

This feature can be modified by use of the DTM. Refer to the sections describing the serial I/O data loop test and the Centronics loopback test (later in this chapter) for more information on LED behavior.

The LED turns solid green when the download is complete and control transfers to the downloaded code. If the cluster controller cannot be downloaded by the host, it remains in the red/green heartbeat pattern. Refer to the *HPS Cluster Controller Download Package User Manual* for more information about downloading the cluster controller.

4.1.3 FLASHING YELLOW

If the LED continues to flash yellow indefinitely, the cluster controller self-test has detected some type of error from which it cannot recover.

4.1.4 FLASHING RED

The LED flashes red during self-test only when a fatal error occurs (that is, other than a failed-port error) and the TO-RST jumper (E2) is installed or an attached DTM is set to 02. The following section addresses how to use the DTM to determine individual test pass/fail status.

4.2 DIAGNOSTIC TEST MODULE

The DTM is a small test "fixture" that SYSTECH developed as a diagnostic aid. With the DTM, you can select special function tests and view the checkpoints and/or error codes as the HPS cluster controller encounters them during self-test or under operating system control.

The DTM, which attaches to the HPS cluster controller board, contains two 16-position rotary switches, two hexadecimal-display LEDs, and a pushbutton switch. The rotary switches select 1 of 256 codes to be read by the cluster controller at power-up (refer to appendix B for the code definitions). The LEDs display the checkpoints or error codes during self-test and error codes during operating system control. Pressing the pushbutton switch resets the HPS cluster controller (this is the equivalent of a power-on reset).

If the rotary switches on the DTM are set to 00 (which is equivalent to not having a DTM attached to the cluster controller), the self-test will reset on an error condition. If the switches are set to 02 or the TO-RST jumper is installed, the self-test will execute as described in this chapter (i.e., on an error condition the cluster controller's LED blinks red and the self-test stops); refer to the code definitions in appendix A. If some other value is entered on the DTM rotary switches, the appropriate action will be taken, as described in appendix B of this manual.

To connect the DTM to the cluster controller board, first remove the six screws securing the cluster controller's plastic cover to the metal base. Lift off the cover and refer to either figure 4-1 or 4-2 to locate the appropriate edge connector for your board. Figure 4-1 identifies the connector as J1 on HPS-7080-030 and HPS-7082-030 cluster controllers; figure 4-2 identifies the connector as J3 on HPS-7088-030 cluster controllers. Connect the DTM to the appropriate connector on your board.

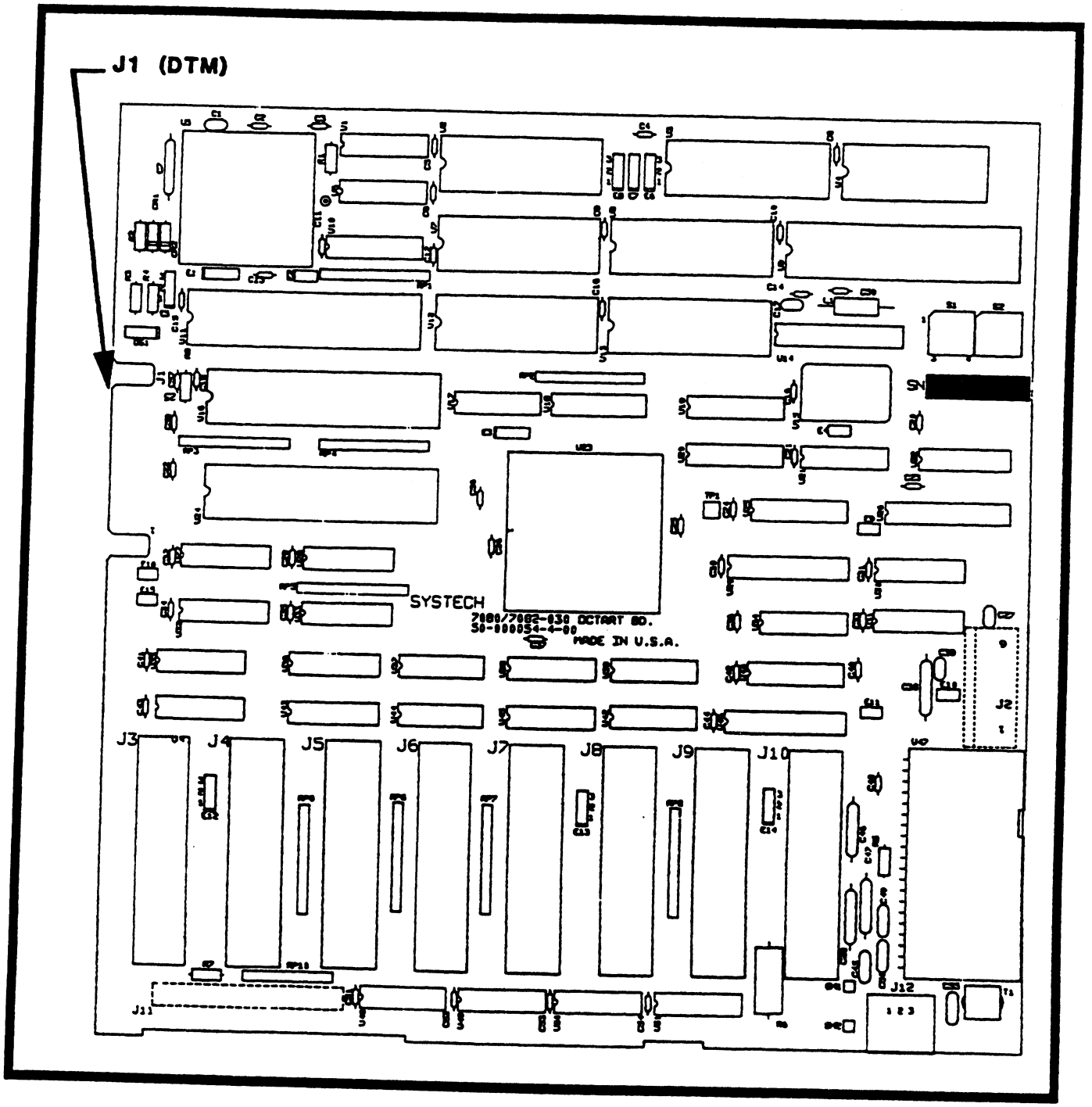


Figure 4-1. DTM Connector on HPS-7080-030 and HPS-7082-030 Cluster Controllers

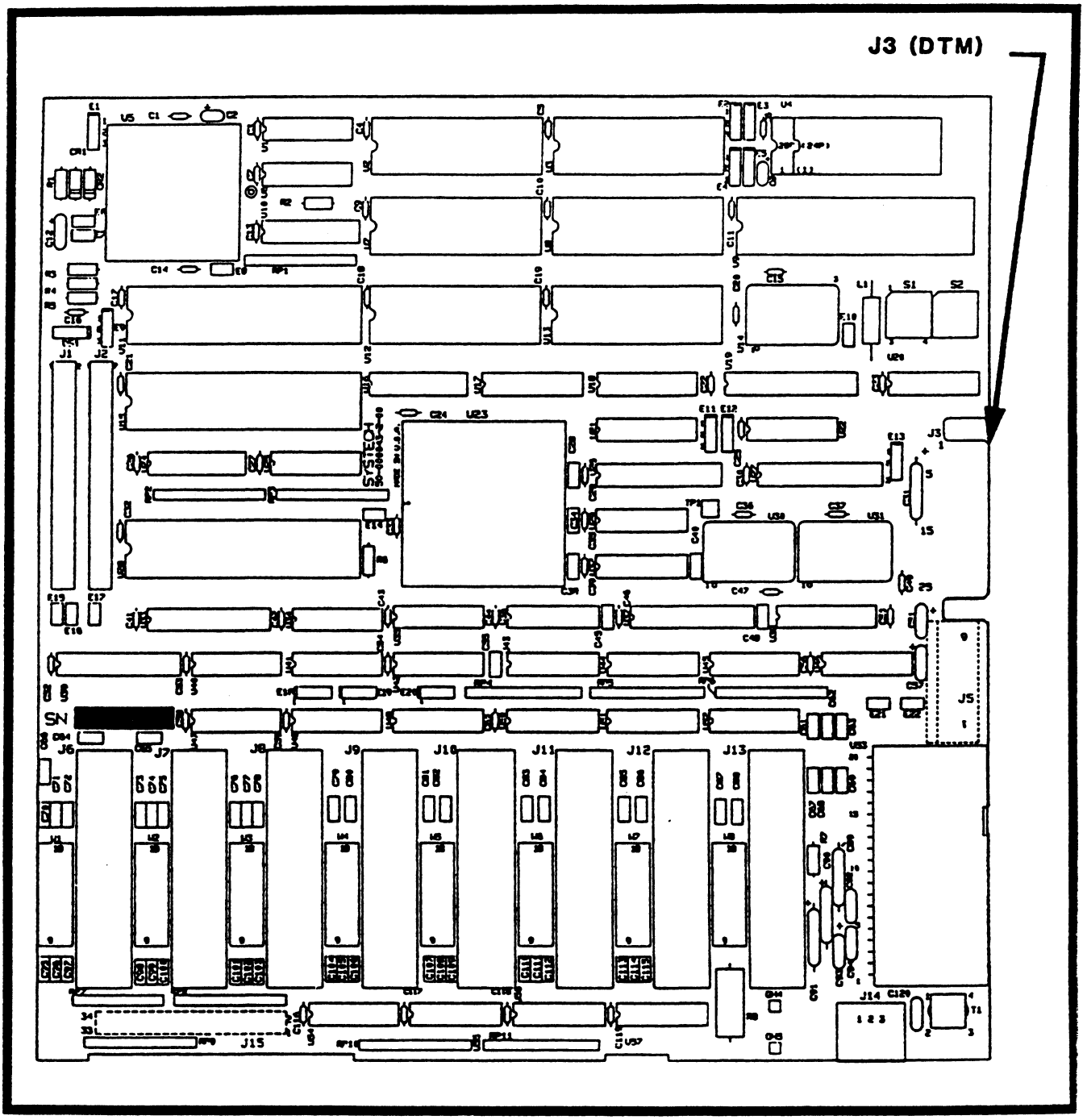


Figure 4-2. DTM Connector on HPS-7088-030 Cluster Controllers

4.3 SELF-TEST ERRORS AND CHECKPOINTS

When an error is encountered during system power-up or reset, an error code or checkpoint value identifying the error code is displayed on the DTM's LEDs.

4.3.1 CHECKPOINTS

Checkpoints are numerical values, each of which corresponds to a particular test or portion of a test. As each test is successfully completed, the appropriate checkpoint is displayed on the DTM (if attached). In this way, you can monitor the tests as they are performed. If an error is encountered that does not allow the cluster controller to display the appropriate error code, the sequence of displaying checkpoints stops, and the last checkpoint identified (corresponding to the last test successfully completed) remains displayed.

Since checkpoints indicate "passed" tests rather than "failed" tests, they do not directly indicate the test on which the error occurred. However, you can deduce the failed test by checking to see which test would have been performed next in the self-test sequence. Appendix C provides a sequential listing of checkpoints and corresponding self-tests.

4.3.2 SELF-TEST ERROR CODES

In addition to checkpoints, error codes can be displayed on the DTM. These codes indicate specifically which test or portion of a test failed. (Refer to appendix D for a sequential listing of the error codes).

4.4 SELF-TEST PROCEDURE

The self-test procedure is described below, along with each error's corresponding error code and checkpoint.

1. **Start of Self-Test**

   The code 00H is displayed on the DTM, indicating that the self-test is ready to begin.

2. **Test for the DTM**

   If the DTM is connected, the rotary switches are read and the appropriate action is taken. Refer to appendix B for DTM commands.

3. **ROM Checksum Test**

   All ROM locations from 0H to 35H and from 38H to the end of EPROM are added, then compared with a precalculated checksum value stored at ROM word location 36H.

   If the values do not match and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 81H** is indicated on the DTM, the cluster controller's LED blinks red, and the self-test stops.

   If no errors are detected, **checkpoint value 01** is indicated.

4. Stack Data Test

The stack tests (4, 5, 6, and 7) check a 256-byte page of on-board RAM starting at absolute address 102000H. This page is used as a processor stack for subsequent portions of the self-test that require a stack, such as the interrupt tests.

The stack location (101FFE) is written with 01, then read back and checked. The bit is then rotated left and checked; this procedure is repeated 15 times to check all the bits.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 82H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 02** is indicated.

5. Stack Address Test

The lower half address of each word location of the stack is pushed onto the stack and then popped off and checked.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 83H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 03** is indicated.

6. Stack Checkerboard Test

All stack locations are first pushed with the value 5555H, and then popped off and checked. Next, all stack locations are pushed with the value AAAAH, and then popped off and checked.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 84H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 04** is indicated.

7. Zero Stack Test

All stack locations are pushed with the value 0000, and then popped off and checked.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 85H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors were detected, **checkpoint 05** is indicated.

8. Stack Addressing Conflicts Test

Various data patterns are written to RAM locations below and above the stack and then the stack is checked for proper data.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 86H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 06** is indicated.

9. Real-Time Clock Test

This is the first time in the self-test where the real-time clock interrupts are enabled.

A delay loop of 200 ms is entered waiting for a real-time clock interrupt. This occurs twice to ensure that the real-time clock interrupt occurs prior to 200 ms elapsing.

If no real-time clock interrupt occurs and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 88H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no real-time clock interrupt occurs during the second delay loop and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 88H** is indicated, the cluster controller's LED blinks red, and the self-test stops

If no errors are detected, **checkpoint 07** is indicated.

10. Real-Time Clock Period Test

The period is checked for 50 ms, ±15% (42.5 ms to 57.5 ms).

If the clock period is out of range and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 89H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 08** is indicated.

11. Data Test/RAM Size

The first word location of each 2000H-byte page is written with a 01H. The bit is checked, then rotated left and checked again. This is done 16 times, until all bit positions of the RAM location have been checked. If an error is encountered and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 8AH** is indicated, the cluster controller's LED blinks red, and the self-test stops.

The size of RAM is determined by adding the number of 2000H-byte pages. This value is saved for future use by the self-test and the operating system. The supported RAM size for the HPS cluster controller is:

100000 to 11FFFF = 128K

If some other size is encountered and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 98H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 09** is indicated.

12. Static RAM Address Test

All RAM locations (except the stack area) are written with a pattern, and then are read and compared. The pattern is one that will detect any address problems that might occur.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 8BH** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 0A** is indicated.

13. Static RAM Checkerboard Test

All RAM locations (except the stack area) are first written with 5555H, and then are read and verified. Secondly, the same locations are written with AAAAH, and then are read and verified.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 8CH** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 0B** is indicated.

14. Zero RAM Test

All RAM locations (except the stack area) are written with 0000H, and then are read and verified.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 8DH** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 0C** is indicated.

NOTE

In the following network RAM tests (15, 16, 17, 18, 19c, and 19d) the network RAM is byte-wide memory. To access network RAM, byte writes/reads are done at odd addresses.

15. Network RAM Data Test

Network RAM, at absolute address location A0005H, is written with 01H. The bit is rotated left and checked. This is done eight times, until all bit positions have been tested.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 8EH** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 0D** is indicated.

16. Network RAM Address Test

All network RAM locations (A0005H through A0FFFH) are written with a pattern, then are read and compared. The pattern is one that will detect any address problems that might occur.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 8FH** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 0E** is indicated.

17. Network RAM Checkerboard Test

First, all network RAM locations (A0005H through A0FFFH) are written with 55H, and then are read and verified. Secondly, the same locations are written with AAH, and then are read and verified.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 90H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 0F** is indicated.

18. Zero Network RAM Test

All network RAM locations (A0005H through A0FFFH) are written with 00H, and then are read and verified.

If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 91H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 10** is indicated.

19. COM 9026 Test

This consists of a series of subtests:

a. The first test makes sure that the COM 9026 chip has a "power-on reset" interrupt pending. If not and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 94H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

b. The COM 9026 status register is then compared for the value E5H. If it is incorrect and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 92H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

c. Byte location A0001H of the network RAM is checked for the value D1H. If this location is incorrect and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 96H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

d. Byte location A0003H of the network RAM is checked for non-zero value. If it is incorrect and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 93H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 11** is indicated (refer to the COM 9026 data sheet for additional information).

20. Serial I/O Data Loop Test

This two-part test, which checks for failed ports, provides two schemes for reporting failures. The first scheme allows this portion of the self-test to pass if some ports fail. The second scheme stops the self-test when the first port error is detected. The reporting schemes are discussed first, followed by a description of the actual tests that are performed by this portion of the self-test.

Scheme 1:

If no DTM is attached, or if a DTM is attached but its switches are set to a setting other than 01 or F0 during this portion of the testing, the self-test will pass if either no ports fail, or if some (but not all) ports fail. If the self-test detects a port failure, the bad port is "remembered" and the next port is tested. At the end of the self-test, the code **FFH** is indicated on the DTM if attached. Then program control and the pass/fail status of all the ports are passed to the operating system.

If an attached DTM is set to 01 and during testing some (but not all) ports fail, **code FEH** is indicated on the DTM at the end of the self-test. Then program control and the pass/fail status of all the ports are passed to the operating system.

If all ports failed and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code B9** is indicated on the DTM, the HPS' LED blinks red, and the self-test stops.

Scheme 2:

If the attached DTM is set to F0, testing will stop when the first port error is encountered. **Error code Ax** is indicated on the DTM, the HPS' LED blinks red, and the self-test stops.

NOTE

Since many error conditions are possible for each port, the displayed error code for a given port indicates only that the port failed, not what caused the failure. The "x" in the error code is replaced by a number indicating which port failed.

In the following descriptions, it is assumed that no self-test errors other than those related to the serial I/O portion of the self-test were encountered. Table 4-1 describes the LED indications that may occur during I/O port testing.

Serial I/O Data Loop Test - Interrupt Loopback Mode

The serial I/O devices are set up as follows:

- character length = 8 bits
- number of stop bits = 1
- parity = none
- baud rate = 9600

In addition, the serial I/O devices will generate transmit (Tx) and receive (Rx) interrupts. This portion of the test performs the following functional checks.

- Data ranging from 00H to FFH is looped through all ports simultaneously. After the Tx and Rx interrupts are enabled, a timeout loop is entered. This loop will wait approximately 1 second for all data to be looped.

  If the timeout occurs before all data has looped, and the conditions for displaying an error code have been met (as described on the previous page), **error code B0H** is indicated, the HPS' LED blinks red, and the self-test stops.

- Continuing with the looped data, after each byte is received, the Rx interrupt routine places the received character into one of the buffers, depending on which port received the data.

- After all data has been looped, it is checked for integrity. (There is one buffer for each DB-25 port on the cluster controller.) The buffers are checked in the following manner:

  - Buffer 0, which contains all the data looped to port 0, contains 256 bytes of incremental data ranging from 00H to FFH.

  - Buffer 1, which contains all the data looped to port 1, contains 256 bytes of incremental data ranging from 01H to 00H.

  - Buffer 2, which contains all the data looped to port 2, contains 256 bytes of incremental data ranging from 02H to 01H.

    •
    •
    •

  - Buffer 7, which contains all the data looped to port 7, contains 256 bytes of incremental data ranging from 07H to 06H.

    •
    •
    •

  - If a sixteen-port cluster controller is being tested, buffer 0FH, which contains all the data looped to port 0FH, contains 256 bytes of incremental data ranging from 0FH to 0EH.

If no errors are detected, **checkpoint 13** is indicated.

Table 4-1. Summary of I/O Port Testing Error Reporting

Number of Failed Ports	Execute Centronics Test ?	Pass Centronics Test ?	DTM Switch Setting = 00		DTM Switch Setting = 01		DTM Switch Setting = F0	
			Displayed DTM Code	LED*	Displayed DTM Code	LED*	Displayed DTM Code	LED*
0	yes	yes	FF	G	FF	G	FF	G
1 - 7	yes	yes	FF	G/R	FE	G/R	Ax	R
8	yes	yes	FF	G/R	FE	G/R	A0	R
0	yes	no	FF	G/R	FE	G/R	E4	R
1-7	yes	no	FF	G/R	FE	G/R	Ax	R
8	yes	no	B9	R	B9	R	A0	R
0	no	–	FF	G	FF	G	FF	G
1-7	no	–	FF	G/R	FE	G/R	Ax	R
8	no	–	B9	R	B9	R	A0	R

* The color/pattern displayed by the cluster controller's LED indicates the following:

G = prior to operating system download, the cluster controller displays an LED pattern whereby the LED is illuminated green, followed closely by a second green, then is off for a period of time before the sequence is repeated (this is referred to as a "heartbeat" pattern); after operating system download, the LED is illuminated solid green.

G/R = green/red combination whereby the LED is first illuminated green, then red, then is off for a period of time before the sequence is repeated; operating system is in control.

R = blinking red; self-test has stopped.

21. Centronics Loopback Test

The following loopback tests are performed only on the model 7082-030 downloadable cluster controller.

This loopback test incorporates a "failed port" error reporting scheme similar to that used for the serial I/O tests. This scheme is described below.

Scheme 1:

If no DTM is attached, or if a DTM is attached but its switches are set to a setting other than 01 or F0, the self-test will pass even if the Centronics test fails. If the self-test detects a failure, the failed port number (port 8) is "remembered" and the next test is executed. At the end of the self-test, code **FFH** is indicated on the DTM if attached. Then program control and the pass/fail status of all nine ports are passed to the operating system.

If an attached DTM is set to 01 and during Centronics testing the Centronics port fails, **code FEH** is indicated on the DTM at the end of the self-test. Then program control and the pass/fail status of all the ports are passed to the operating system.

If all ports failed and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code B9** is indicated on the DTM, the HPS' LED blinks red, and the self-test stops.

Scheme 2:

If the attached DTM is set to F0, Centronics testing will stop when the first error is encountered. **Error code E4** is indicated, the cluster controller's LED blinks red, and the self-test stops. Refer to table 4-1 for a description of the LED indications.

Prior to performing the data loop tests discussed below, the self-test checks the Centronics ASIC's internal registers. If an error is detected, the appropriate action is taken, based on the reporting scheme you have selected (as described previously).

Centronics Data Loop Test, Part 1 - Polled Loopback Mode

Data ranging from 00H to FFH is written to the Centronics port one byte at a time. After each byte has been written, it is read back from the Centronics port and verified.

If an error is detected, the appropriate action is taken, based on the reporting scheme you have selected (as described previously).

If no errors are detected, **checkpoint 14** is indicated.

Centronics Data Loop Test, Part 2 - Interrupt Loopback Mode

- A data pattern consisting of 256 bytes is written, under interrupt control, to the Centronics port. The data is looped through the Centronics port and read back, under interrupt control, into a buffer. The data in the read buffer is checked for integrity.

  If an error is detected, the appropriate action is taken, based on the reporting scheme you have selected (as described previously).

- A series of tests is performed to test the Centronics interface signals.

  If an interface signal error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code E4H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

  If no errors are detected, **checkpoint 15** is indicated.

22. Clear all RAM

All RAM (except the stack area) is cleared to zero.

If an error is detected while clearing RAM and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 97H** is indicated, the cluster controller's LED blinks red, and the self-test stops.

If no errors are detected, **checkpoint 16** is indicated.

23. Burn-In Loopback/Termination

If the burn-in mode was previously selected (DTM rotary switches set to FFH), the self-test will start over from the beginning and keep repeating.

The cluster controller is set up for control to be passed to the operating system. Part of this setup includes enabling the RAM memory map into RAM. If an error is detected and the attached DTM's rotary switches are set to 02 or the TO-RST jumper is installed, **error code 95** is indicated, the cluster controller's LED blinks red, and the self-test stops.

At this point, depending on the conditions described below, either code **FFH** or code **FEH** is indicated on the DTM if attached. In most instances, code **FFH** will be indicated. Code **FEH** is indicated only if a DTM is connected, the DTM's rotary switches are set to 01H, and one or more--but not all--of the cluster controller's ports failed during the OctART testing.

No error code or checkpoint is associated with this function. The self-tests are complete at this point and control is passed to the operating system.

NOTE

Refer to appendix B for a detailed explanation of burn-in mode.

The self-tests are complete at this point, and the cluster controller is ready for operating system download.

Chapter 5
OEM Warranty and Repair Procedure

This chapter explains how to contact SYSTECH's Customer Service Product Support group regarding product operating problems, and describes how to return products for repair (both warranty and nonwarranty products).

This information applies to SYSTECH's authorized distributors (OEMs). An "end user's" point of contact for support or repair is the authorized distributor from which the product was purchased.

For reference, the SYSTECH Corporation warranty appears at the end of this chapter.

5.1 CALLING CUSTOMER SERVICE

Before calling the customer service number regarding a product support issue, have the following information available:

- A detailed description of the problem.
- System type.
- Operating software and version level.
- SYSTECH product, model, part number, and revision level.

The SYSTECH customer service number is: **(619) 453-8976**

5.2 RETURNING PRODUCT FOR REPAIR

Should the product need to be returned for repair, you will need a Return of Material Authorization (RMA) number from SYSTECH. The RMA number is valid for 30 days. All returns to the factory (warranty, nonwarranty, loaners, evaluation, beta, and exchanges) require an RMA number. The RMA number must appear on the outside packaging of all returned products.

A valid purchase order is required for all repaired products, both warranty and nonwarranty. Products under warranty will be returned prepaid; products not covered under warranty will be returned prepaid and billed.

NOTES

Any parcel received without an RMA number noted on the outside of the package will be refused by the SYSTECH receiving department, and will be returned freight collect to the sender.

For international shipments, we do not recommend the use of Air Parcel Post.

To return product for repair:

- Obtain an RMA number by calling the SYSTECH order entry department at (619) 453-8970.
- To enable us to verify warranty repairs, provide to our order entry representative the date you received the product.
- Provide a valid purchase order number for the product being returned.

- Provide the part number and serial number of the SYSTECH product. For most board assemblies, the serial number is located on the component side while the part number is printed on a small white label on the solder side (the part number takes the form 65-xxxxxx-x-xx). For cluster controllers and SPURs, the serial number is on a large silver label and the part number (65-xxxxxx-x-xx) is on a small white label; both are affixed to the bottom of the unit.

- Verify with the order entry representative your shipping and billing address.

- Describe the problem and include the name and phone number of a technical contact who can provide further information about the failure.

- Package the product for shipment, indicating on the outside of the parcel the RMA number. Then ship the product freight and insurance prepaid to:

  SYSTECH Corporation
  6465 Nancy Ridge Drive
  San Diego, CA 92121

- The product will be returned, repaired or exchanged within 30 working days. A valid hardcopy purchase order must be received by SYSTECH before the product will be returned to the customer. Products under warranty are returned prepaid. Products not covered under warranty are returned prepaid and billed.

5.3 SYSTECH CORPORATION WARRANTY

1. **WARRANTY:** SYSTECH Corporation ("Company") warrants that hardware products manufactured by it are free from defects in materials and workmanship under normal conditions of usage and service for a period of one year from the date the product is shipped from Company's factory. This warranty shall not apply to any product which was repaired or altered outside of Company's factory or authorized service stations, nor which has been subject to misuse, negligence or accident, or use not in accord with instructions furnished by Company.

2. **RETURN OF DEFECTIVE PRODUCT:** Purported defective products shall be properly packaged by Buyer and shipped, insured, at Buyer's cost to one of Company's authorized service stations for verification of defects.

3. **REPAIR OR REPLACEMENT:** If after examination, Company determines that a product is defective, Company shall, at its option, replace or repair the product at no cost to the Buyer. Return of the repaired or replaced defective product to Buyer shall be at Company's expense. Company warrants any repair or replacement for 30 days or remainder of original warranty, whichever period is longer.

4. **PRODUCTS NOT SUBJECT TO WARRANTY:** Buyer shall pay all transportation charges plus Company's established price for replacement or repair of products sent to Company by Buyer for replacement or repair outside the scope of the warranty.

5. **DISCLAIMER AND LIABILITY RESTRICTION:** THERE ARE NO WARRANTIES EXPRESS, IMPLIED, OR ARISING BY OPERATION OF LAW, EXCEPT THOSE SET FORTH HEREIN, AND THE LIMITATION OF OBLIGATION HEREIN DESCRIBES THE SOLE AND EXCLUSIVE DUTIES, OBLIGATIONS AND RIGHTS OF COMPANY, BUYER, AND THEIR SUCCESSORS.

   IN NO EVENT, BE IT DUE TO A BREACH OF ANY WARRANTY HEREUNDER OR ANY OTHER CAUSE WHATSOEVER, SHALL COMPANY BE LIABLE FOR OR OBLIGED IN ANY MANNER TO PAY CONSEQUENTIAL OR INDIRECT DAMAGES, INCLUDING, BUT NOT LIMITED TO, LOSS OF PROFITS, PLANT DOWNTIME, PROPERTY DAMAGE, OR PERSONAL INJURY DAMAGE ASSERTEDLY SUFFERED BY BUYER OR THIRD PARTIES WHETHER SUCH CLAIM IS BASED ON CONTRACT OR TORT.

   The warranty contained herein, including the Disclaimer and Liability Restriction, constitutes the entire agreement of Company and Buyer with respect to such matters, supersedes and is a merger of all prior negotiations and shall be controlling over any conflicting terms and conditions of any contracts, purchase orders, invoices, or the like, which are or may be executed in connection with the attached contract. If this warranty is voided by any breach of Condition, the Disclaimer and Liability Restriction shall remain fully effective.

   No agent, employee or representative of Company has any authority to bind Company to any affirmation, representation or warranty concerning any goods, services or processes other than set forth herein.

6. **ASSIGNMENT:** This warranty may not be assigned or otherwise transferred by Buyer without the prior written consent of Company; provided, if Buyer advises Company in writing at the time of purchase that the product has been bought for resale, Buyer may assign this warranty to its customer.

7. **LIABILITY LIMITATIONS:** If at any time there shall be any liability asserted against Company for goods, services or processes furnished under this Agreement, notwithstanding the foregoing limitations and waivers, Buyer agrees to indemnify Company, hold it harmless and defend it against all liabilities from loss, damage or injury to persons or property by reason of the use of any goods, services or processes provided under this Agreement, regardless of cause or responsibility for negligence.

8. **LIMITATIONS OF DAMAGES OR REMEDIES:** In the event the provisions disclaiming warranties relieving Company from liability for its negligence should, for any reason, be held ineffective, it is expressly agreed that replacement and repair shall be the sole remedy of Buyer with respect to any other remedy available by applicable law.

Appendix A
DTM Rotary Switch Code Definitions

A.1 HOW TO USE THE DTM

To execute a function on the Diagnostic Test Module (DTM), enter, on the DTM's two rotary switches, the code associated with that function (the codes are defined below). Then press the DTM's RESET button.

At this point, if the function is a test or scope loop function, the desired action will continue until a new code is entered and the RESET button is pressed again.

If the desired function is a mode type function, the self-test will execute as described in chapter 5, with the exception of the change associated with the DTM code.

NOTE

Invalid codes (that is, any that are not listed and defined below) are handled in the same manner as a setting of 00.

A.2 CODE DEFINITIONS

The DTM codes and their corresponding definitions are listed below.

- **00** = This is the default value. Enter this code if no test or mode is desired.

- **01** = **Display Serial I/O Test Status**

  At the completion of self-test, the code FEH will be displayed on the DTM if one or more--but not all--ports failed during the serial I/O portion of the testing, and/or the Centronics portion of the self-test fails (the Centronics test is applicable only for models 7082-030).

  If all ports passed the serial I/O portion of the self-test, the code FFH will be displayed on the DTM.

- **02** = **Watchdog Timeout/Reset**

  Operates as does the default value (00) except that the watchdog timeout/reset is disabled. The cluster controller won't reset, and an error code will be displayed.

- **20 - 2F** = **Serial I/O Device Output Loop**

  This scope loop verifies (with the aid of an oscilloscope) that the TxDATA line and the output modem control signals for a selected port can change state from a high to a low level. The port is the lower nibble of the 2x number entered on the DTM rotary switches.

  The serial I/O device is set up for 9600 baud, no parity, eight data bits, and one stop bit.

  The data pattern 55H AAH is sent out the TxDATA line, and is also sent to the serial I/O device's modem control signal output port.

If an invalid DTM code is entered (such as 28H through 2FH for an eight-channel multiplexer), an error code will be displayed on the DTM's LEDs.

To stop this test, either change the channel number or continue after an error. If you choose to continue, enter 00 or a new DTM code on the DTM's rotary switches, then press the DTM's RESET button.

- **30** = **DTM Test**

  This test verifies the DTM and interface circuitry.

  The code entered on the DTM's rotary switches will be displayed on the DTM's LEDs.

  To stop this test, enter 00 or a new DTM code, then press the DTM's RESET button.

- **31** = **Serial Data External Loop Mode**

  This mode sets up the serial I/O device to send the serial data, during the serial I/O portion of the self-test, to the RS-232 connectors' TxDATA serial lines.

  For the serial I/O test to successfully complete, you must install a jumper between TxD and RxD on each port.

  If an error is detected during the serial I/O portion of the self-test with this mode enabled, error code **Ax** is displayed on the DTM, the HPS' LED blinks red, and the self-test stops.

  Since this is a DTM mode command, after the serial I/O test has been completed, the remainder of the self-test completes as described in chapter 5 of this manual.

- **40** = **COM Address Test**

  This test verifies that the COM address switches and interface circuitry function properly. The number displayed on COM address switches S1 and S2 is displayed on the DTM's LEDs. As the address switches are rotated, the DTM's LEDs display the new address.

  When this test is finished, the COM address must be set to a nonzero value for the self-test to successfully complete.

  To stop this test, enter 00 or a new DTM code on the DTM's switches, then press the RESET button.

- **50** = **Centronics Port Test**

  This test sends ASCII data to the Centronics port. The ASCII data is incremental from 21H to 6FH. The pattern is repeating.

  To stop this test, enter 00 or a new DTM code on the DTM's switches, then press the RESET button.

- **F0** = **Stop Self-Test on First Failed Port**

  This mode cancels the "failed port" mode by not allowing program control to be passed to the operating system if a failed port is indicated.

  When a failed port is detected during the serial I/O portion of the self-test, error code **Ax** is displayed on the DTM, the HPS' LED blinks red, and the self-test stops.

  If, during testing of a model HPS-7082-030, the Centronics portion of the self-test fails, error code E4 is displayed on the DTM, the HPS' LED blinks red, and the self-test stops.

- **FD = Display Last Error Encountered**

  While not actually a mode or a test, this function will only be performed if the "burn-in mode" (described below) was previously selected (DTM's rotary switches set to FFH). This function displays the last error that was encountered during continuous execution of the self-test.

  After selecting this function, do not press the DTM RESET button to invoke it. The error code display may take several seconds to appear because the current self-test loop must complete before the error code can be displayed.

  If no errors were previously detected, the DTM's LEDs will display 00. If an error was detected, the DTM's LEDs will alternate between 00 and the error code.

  To continue the burn-in mode, rotate the DTM's rotary switches back to FFH.

- **FE = Display Total Count of Errors**

  While not actually a mode or a test, this function will only be performed if the burn-in mode was previously selected (DTM's rotary switches set to FFH). This function displays the total number of errors that have been encountered during continuous execution of the self-test.

  When this function is selected, do not press the DTM RESET button to invoke it. The error count display may take several seconds to appear because the current self-test loop must complete before the count can be displayed.

  If 255 or more errors have been detected, the DTM's LEDs will display FFH.

  To continue the burn-in mode, rotate the DTM's rotary switches back to FFH.

- **FF = Burn-In Mode**

  This mode differs from the other modes in that after rotating the DTM's rotary switches to the FFH position, you must press the DTM's RESET button to start executing the continuous self-test. Once you've initiated the self-test, you must refrain from pressing the RESET button again.

  This mode executes the self-test repeatedly, keeping track of the last error and the total error count.

  If an error is detected, the LED located on the HPS cluster controller will blink red (instead of yellow). This indicates that an error has occurred, and by using the DTM's "error type" and "error count" functions (described above), you can determine the error type and frequency of errors.

  To stop this test, enter 00 or a new DTM code, then press the DTM's RESET button.

Appendix B
Self-Test Checkpoints

The checkpoints recognized by the HPS cluster controller self-test software (and described in chapter 5) range in value from 01H to 7FH. The checkpoints are listed below, along with a brief description of what each checkpoint indicates.

- **00** = Reset condition. The HPS cluster controller is starting the self-test operation.
- **01** = ROM checksum test was completed successfully.
- **02** = Stack data test was completed successfully.
- **03** = Stack address test was completed successfully.
- **04** = Stack checkerboard test was completed successfully.
- **05** = Zero stack test was completed successfully.
- **06** = Stack addressing conflicts test was completed successfully.
- **07** = Real-time clock test was completed successfully.
- **08** = Real-time clock period test was completed successfully.
- **09** = Data/RAM size test was completed successfully.

- **0A** = Static RAM address test was completed successfully.
- **0B** = Static RAM checkerboard test was completed successfully.
- **0C** = Zero RAM test was completed successfully.
- **0D** = Network RAM data test was completed successfully.
- **0E** = Network RAM address test was completed successfully.
- **0F** = Network RAM checkerboard test was completed successfully.
- **10** = Zero network RAM test was completed successfully.
- **11** = The COM 9026 tests were completed successfully.
- **13** = The Serial I/O Interrupt Loopback Mode test was completed successfully.
- **14** = The Centronics Option Polled Loopback Mode test was completed successfully.
- **15** = The Centronics Option Interrupt Loopback Mode test was completed successfully.
- **16** = Zero RAM test was completed successfully.
- **FF** = Entire self-test was completed successfully.

Appendix C
Self-Test Error Codes

The error codes recognized by the HPS self-test software (and described in chapter 5) range in value from 80H to FFH. The error codes are listed sequentially below, along with a brief description of the test that corresponds to each error code.

- **80** = Not used at this time.
- **81** = ROM checksum error.
- **82** = Stack data test error.
- **83** = Stack address test error.
- **84** = Stack checkerboard test error.
- **85** = Zero stack test error.
- **86** = Stack addressing conflicts error.
- **87** = Not used at this time.
- **88** = Real-time clock interrupt error (no real-time clock present).
- **89** = Real-time clock interrupt error (bad clock pulse width).

- **8A** = Static RAM data test error.
- **8B** = Static RAM address test error.
- **8C** = Static RAM checkerboard test error.
- **8D** = Zero RAM test error.
- **8E** = Network RAM data test error.
- **8F** = Network RAM address test error.
- **90** = Network RAM checkerboard test error.
- **91** = Zero network RAM test error.
- **92** = COM 9026 status register value error.
- **93** = COM 9026 network ID test error.
- **94** = COM 9026 power-on reset test error.
- **95** = RAM map error.
- **96** = COM 9026 source ID error.
- **97** = Zero static RAM test error.
- **98** = Invalid static RAM size error.
- **Ax** = Serial port "x" failed during the serial I/O test. The failed port "x" is 0 to 7 for the eight-port cluster controller, or 0 to F for the sixteen-port cluster controller.
- **B0** = Serial I/O interrupt loopback timeout error.
- **B2** = Spurious network interrupt.
- **B9** = All ports failed during the serial I/Os portion of self-test (applies only to downloadable cluster controllers).
- **E4** = Centronics option data loop error.

NOTE

Error codes F0 through F5 are discussed further in the Motorola publication, *MC68000 16/32-Bit Microprocessor Programmer's Reference Manual*, available from your Motorola representative.

- **F0** = Bus exception error.
- **F1** = Address exception error.
- **F2** = Illegal instruction error.
- **F3** = Interrupt exception error.
- **F4** = Trap exception error.
- **F5** = Other exception error.

Appendix D
Response Control Capacitors for HPS-7088-030

The HPS cluster controller was designed so that capacitors can be added to either control the slew rate of the driver to meet RS-232 and CCITT, V.24 specifications or to filter any potential incoming high-frequency noise pulses. This appendix explains how to add capacitors for these two purposes.

With the advent of the more modern serial USART controllers in use today, these filter capacitors are not normally used, however, they can be installed to satisfy particular applications.

D.1 CONTROLLING THE SLEW RATE

Recommendations for RS-232C specification state that during transitions, the driver output slew rate should not exceed 30 volts per microsecond. The inherent slew rate of an unloaded 75188/1488 driver (figure D-1) is much faster and, if needed, the rate can be controlled by connecting a capacitor to the output of each driver. The value of the capacitors used depends largely on the length and type of serial cable used. Because you determine these factors, you must also select the capacitor values to be used.

The required capacitance can be determined by the following equation:

Capacitance = Isc (short circuit current) x change in time / change in voltage

Figure D-2 shows the slew rate before capacitors are added, with a 10 mA current. As indicated, a 330 pF capacitor could be used to achieve the desired slew rate.

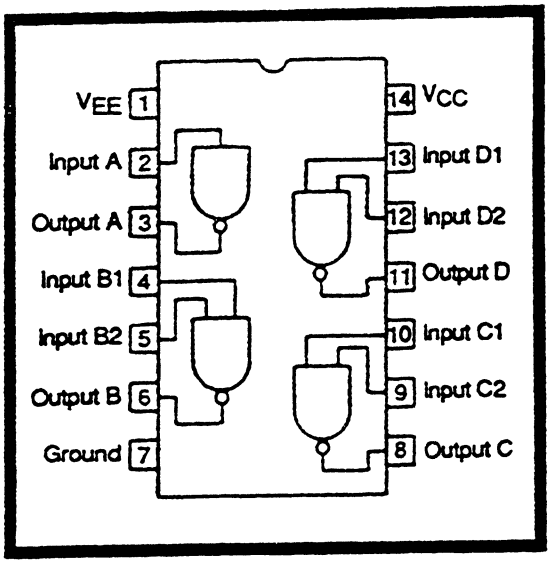


Figure D-1. 75188/1488 Pin Connections

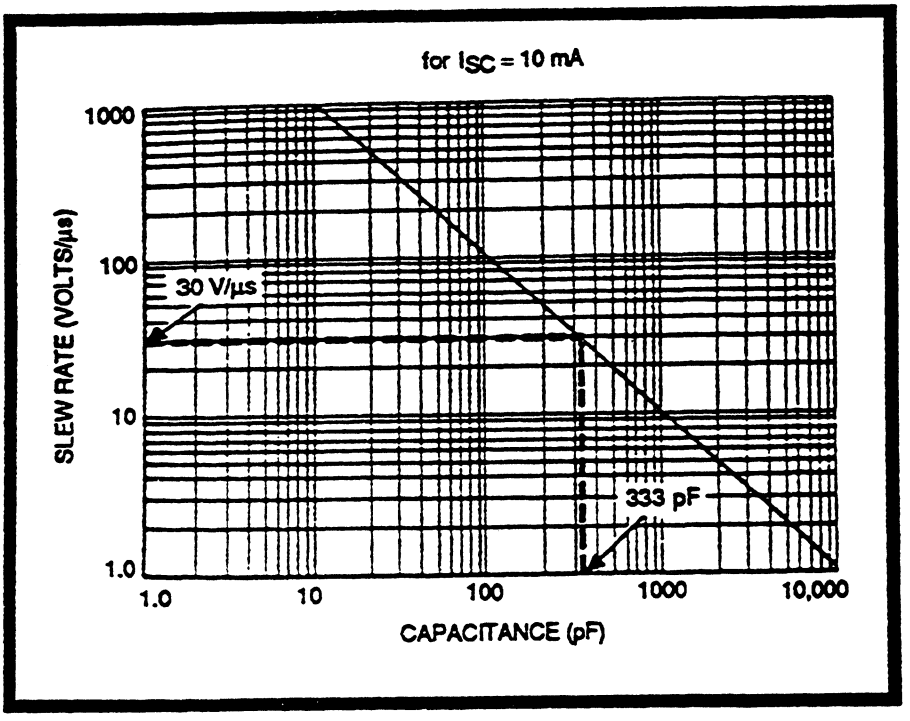


Figure D-2. Slew Rate Versus Capacitance

D.2 FILTERING NOISE PULSES

You can add capacitors to the response control pins of the 75189/1489 and 75189A/1489A to filter high-frequency noise pulses. The value of the capacitors used depends largely on the desired baud rate and the amount of filtering desired. Because you determine these factors, you must also select the capacitor values to be used. A 75189/1489 receiver (figure D-3) contains inputs called "response control." These pins can be used to filter high-frequency noise pulses. Figures D-4 and D-5 show typical noise rejection for capacitors of various sizes. The circuit schematics of the 75189/1489 are shown in figure D-6.

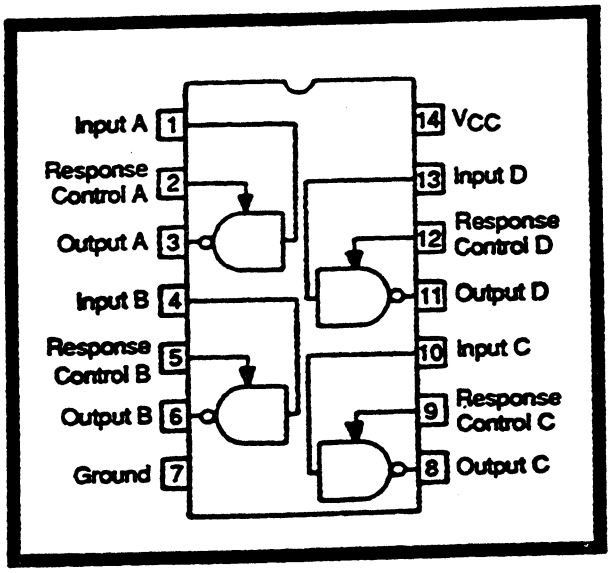


Figure D-3. 75189/1489 and 75189A/1489A Pin Connections

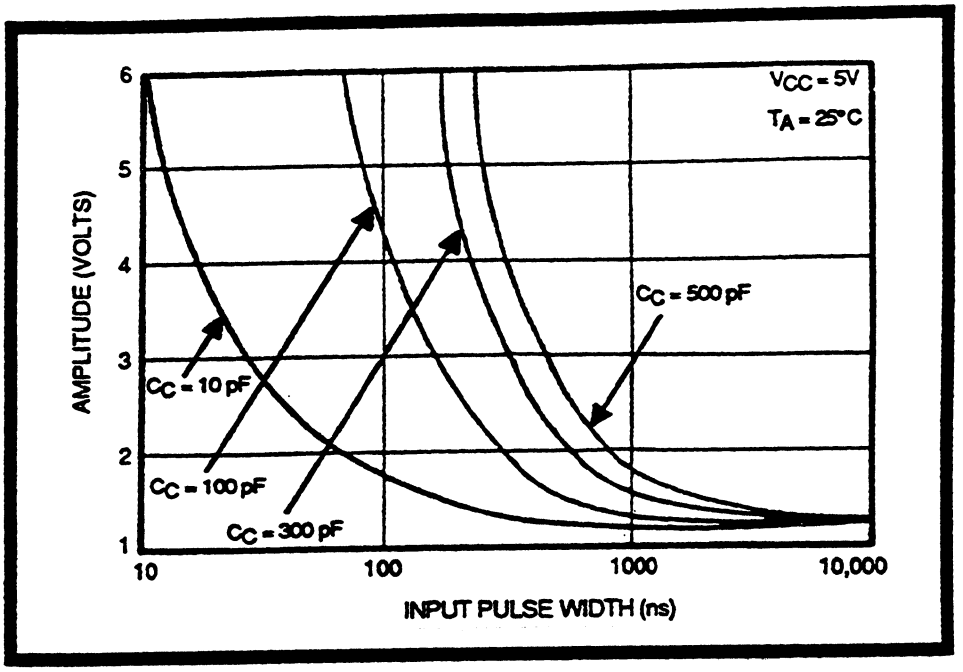


Figure D-4. 75189/1489 Noise Rejection

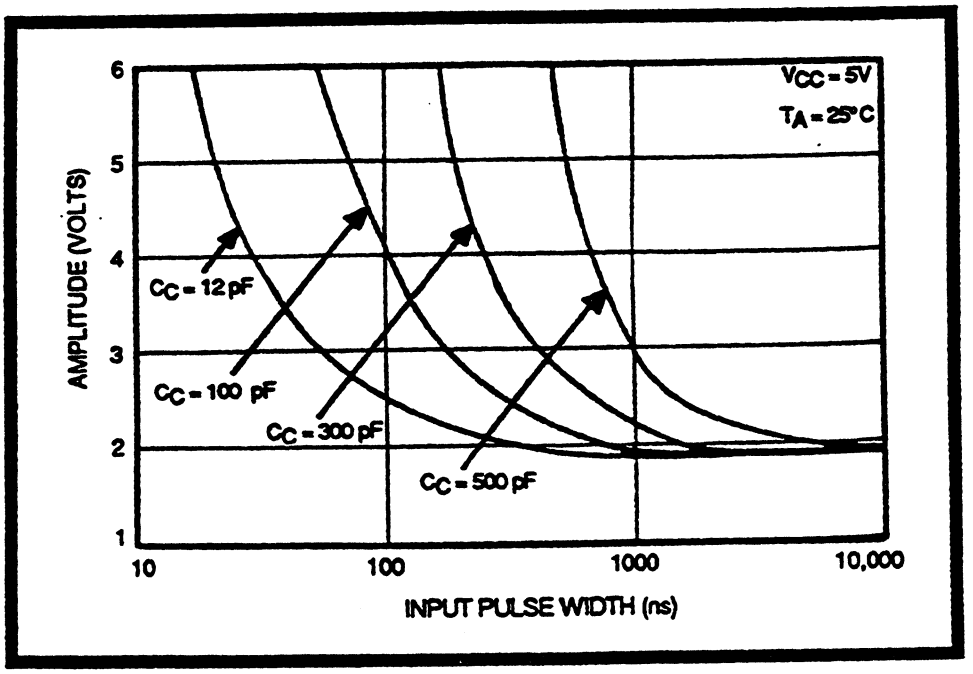
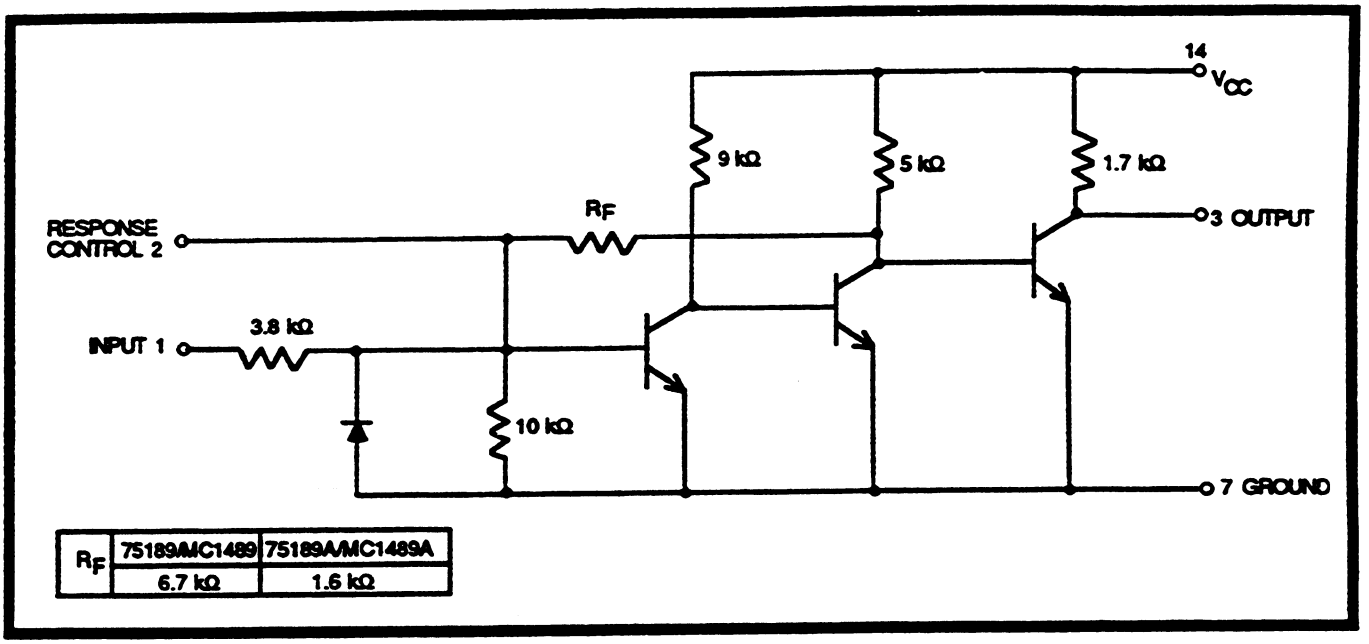


Figure D-5. 75189A/1489A Noise Rejection



R_F	75189/MC1489	75189A/MC1489A
	6.7 kΩ	1.6 kΩ

Figure D-6. 75189/1489 Circuit Schematic

December 12, 1990

Erratum

This erratum affects revision C of the *HPS Model 030 Cluster Controller Technical Manual*, SYSTECH part number 80-000664-4-00.

Electrical specifications for the HPS-7082-030 parallel printer interface were added to chapter 3, and affected pages of the table of contents were corrected and included in the erratum package.

A new title page, with a "change record page" printed on the back, has been included in this erratum. The change record page is for your reference; it identifies the changes made to the manual.

To incorporate the erratum into your manual, replace the manual's title page/change record page (located immediately behind the cover sheet) with the corresponding new page. Then replace the existing (old) pages with the revised pages from the erratum package; the footer at the bottom of each new page identifies it as containing a change.

HPS Model 030
Cluster Controller
Technical Manual

(80-000664-4-00 Revision C)

HPS Model 030
Cluster Controller
Technical Manual

United States Patent Number 4,845,609

Change Record Page

Manual Part No. 80-000664-4-00

Date	Rev	By	Description	Pages Affected
1/5/88	A	ELB	Initial release.	All
2/9/89	erratum	ELB	Added Canadian DOC notice; added parallel printer signal information (chapter 2).	iii, vi, 1-10, 2-3, 2-4, 2-5
7/25/89	B	ELB	Incorporated 2/9/89 erratum; added HPS-7088-030 information; revised regulatory agency information.	iii – vi, 1-1, 1-3 – 1-14, 2-1 – 2-6, 3-2, 3-19, 4-3 – 4-20, D-1 – D-5
10/5/89	erratum	ELB	Added note about using proper power cord for AC voltage applied; corrected product weights listed in table 1-2; removed erroneous model number from appendix A.	1-13, A-4
6/6/90	C	ELB	Incorporated 10/5/89 erratum; clarified section 1.5.2 and the power requirements (table 1-2); revised the warranty and repair information.	v, 1-11, 1-13, 5-1 – 5-4, A-4
12/12/90	erratum	ELB	Added parallel printer electrical interface specifications.	iv, vi, 1-14, 3-15 – 3-20

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1.7 SPECIFICATIONS

Table 1-2 lists the specifications for model 030 downloadable cluster controllers.

NOTE

Model 030 cluster controllers are equipped with auto-ranging input circuitry suitable for 120 VAC and 220 VAC operation. No adjustments are necessary. Be sure to use the proper power cord for the AC voltage applied.

Table 1-2. HPS Cluster Controller Specifications

Parameter	Specification
Dimensions	**HPS-7080-030** and **HPS-7082-030**: 2-7/8 in. high by 10-1/8 in. wide by 10 in. deep (7.3 cm high by 25.7 cm wide by 25.4 cm deep) **HPS-7088-030**: 2-7/8 in. high by 20-5/8 in. wide by 10 in. deep (7.3 cm high by 52.4 cm wide by 25.4 cm deep)
Weight	**HPS-7080-030**: 3.57 lb (1.62 kg) **HPS-7082-030**: 3.68 lb (1.67 kg) **HPS-7088-030**: 6.59 lb (2.99 kg)
Power requirements	120V/240V (92 – 249 VAC, 0.5A – 0.4A, 47 – 63 Hz)

Table 1-2. HPS Cluster Controller Specifications (Continued)

Parameter	Specification
Environment	operating temperature: 0°C to 40°C (ambient) 32°F to 104°F (ambient)
	operating humidity: 10% to 90% noncondensing
	storage temperature: 0°C to 55°C (32°F to 131°F)
Processor	10 MHz 68000
Serial I/O interface	RS-232C
Signals supported	TXD, RXD, RTS, CTS, DTR, DSR, DCD, and Ground
Transport protocol	Token-passing bit serial bus system
Transport interface	2.5 Mbit high-impedance transceiver
Transport medium	RG-62A/U, 93 ohm coaxial cable terminated at each end with 93 ohm passive terminators
Maximum transport length	1000 foot maximum network length, without the use of HPS SYSTECH Pluriaxial Unplug Repeater (SPUR) units
Indicators	Tri-color status light-emitting diode (LED)
Printer port	HPS-7082-030 only: Centronics-type parallel printer port

3.3.7 NET I/O/NET MEM WRITE CYCLE

At the beginning of a NET I/O/NET MEM write cycle (during S1), the microprocessor places the desired NETI/O or NET RAM byte on the local address bus (LA1 through LA23). During S2, the address strobe is asserted, indicating that a valid address is on the address bus. After the trailing edge of S2 "falls," data is asserted on the local data bus (LD0 through LD7). The microprocessor asserts the data strobe 20 ns or more after the data is asserted, indicating that valid data exists on the data bus. The net memory block is decoded by the REM1. *NETSEL/* enables a wait-state flip-flop to provide an input to the DTACK circuit (after *NETWAIT* goes true, or low) to begin terminating the NET I/O/NET MEM write cycle. *NET MEM/* and *NET I/O/* also enable the COM 9026.

The COM 9026 controls all CPU access to itself and to its 2K x 8 SRAM. As *NETI/O* or *NET MEM* is asserted to the COM 9026, it responds by raising its *NETWAIT* output. The CPU, seeing no *DTACK/* from the net, enters a wait state. It continues to wait until the COM 9026 drives the *NETWAIT* signal low, causing the net wait flip-flop to declare *DTACK/*. Note that this may happen up to 1.3 µs later. *DTACK/* causes the microprocessor to begin completing the cycle. During this time, the microprocessor places valid data on LD0 through LD7. The COM 9026 routes and writes the data to its destination. As the microprocessor cycle completes, the data strobe terminates; the address strobe also terminates, which in turn terminates the NET I/O/NET MEM selection and ultimately, the write cycle.

3.3.8 HPS-7082-030 INTERFACE

3.3.8.1 Printer Interface Timing Specifications

The HPS-7082-030 supports a Centronics-type printer interface. The printer data setup time is 600 ns, followed by a printer data strobe of 800 ns. The data hold after strobe is longer than 1 µs, because the data is held until the next printer data write cycle. This time is dependent on the microprocessor print data intercharacter processing, microprocessor speed, and other processing functions handled by the microprocessor between print characters. The printer interface timing diagram appears as figure 3-4.

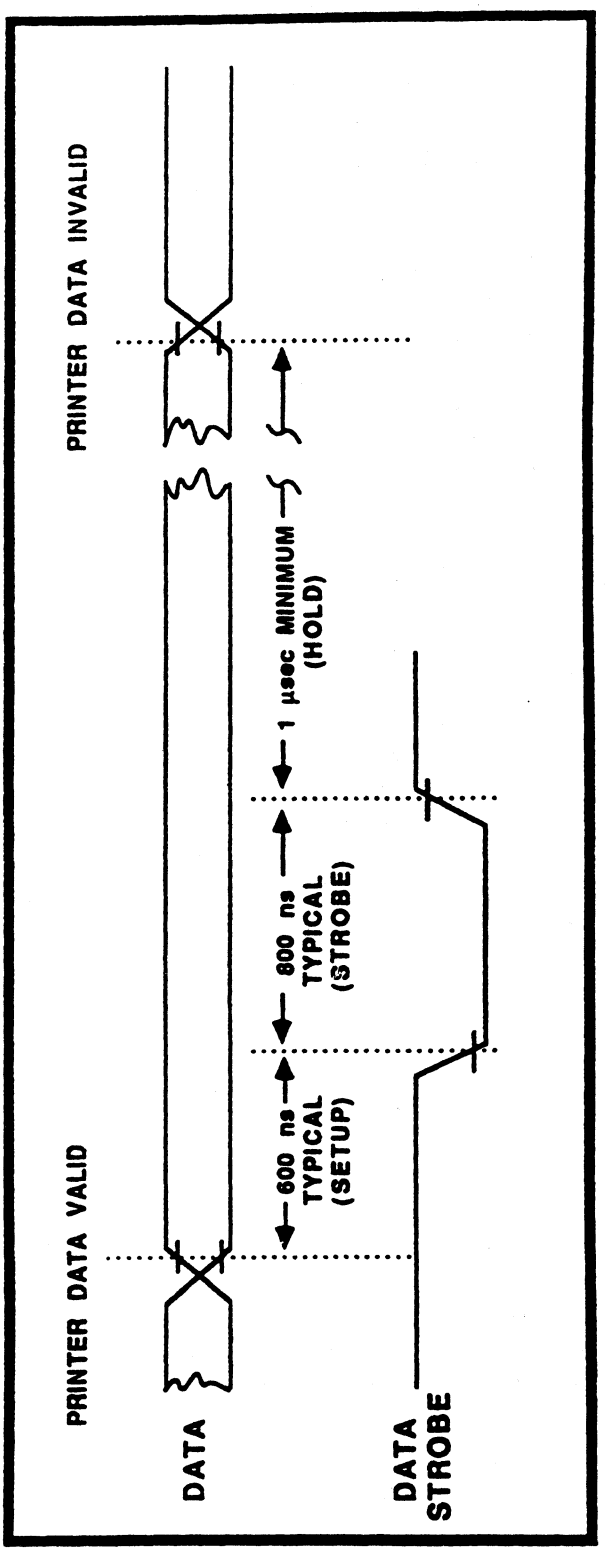

Figure 3-4. HPS-7082-030 Printer Interface Timing Diagram

3.3.8.2 Printer Electrical Interface

The Centronics electrical interface design is described below and illustrated in figure 3-5. A parallel printer with the same type of interface will operate properly at a distance of 25 feet from the cluster controller. To determine the maximum distance that a particular printer may be located from a cluster controller, use the interface specifications provided to calculate an acceptable distance.

- Input characteristics: Each input pin from the printer connector is terminated with a 220 ohm pull-up and a 330 ohm pull-down circuit, followed by a 10k-ohm series resistor. This provides a noise-free low-impedance input.

  - V_{il} = 0.8V at I_{il} of -16.7 mA or more negative
  - V_{ih} = 2.4V at I_{ih} of -4.5 mA or more positive

- Output characteristics: Each output to the printer connector is driven with 1k-ohm pull-up open collector driver. This provides high drive capability plus protection against short circuits.

  - V_{ol} = 0.4V at I_{ol} of 40 mA or less

3.3.8.3 Printer Interface Registers

The printer interface has seven internal registers, as listed in table 3-1 and described below.

- **Printer data register**

  The printer data register is used for writing data to the printer. If a sample of what was written to the printer is desired, the printer data register can be read. Reading the printer data register will not create a data strobe to the printer.

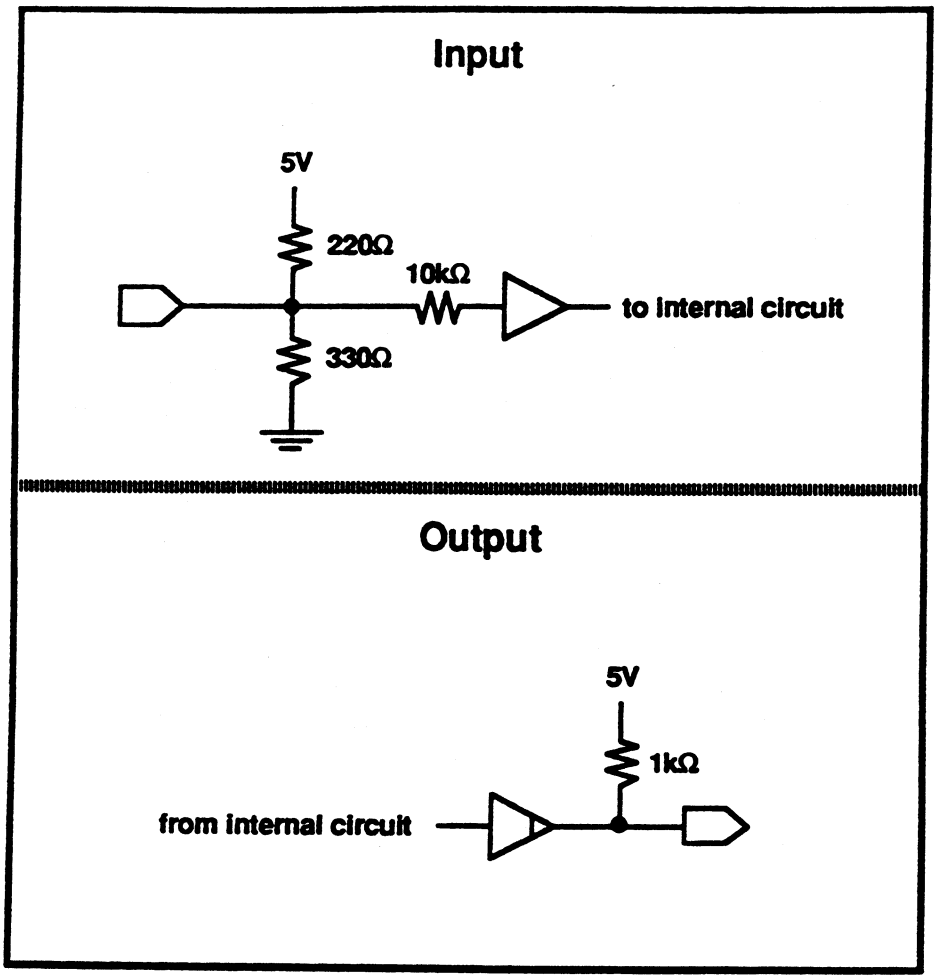

Figure 3-5. HPS-7082-030 Printer Electrical Interface

- **Configuration register**

  The configuration register is used for programming the operating configuration of the printer port. If verification of the configuration is desired, the configuration register can be read.

- **Interrupt register**

  The interrupt register is a monitor of all items in the printer/printer interface which may need attention. There is no access for writing to the interrupt register, so the only way to clear an interrupt is to either mask it in the configuration register or service the interrupt.

- **Loopback Configuration Register**

  The loopback configuration register provides a means to loopback test the logic within the printer I/O option.

Table 3-1. Printer Interface Registers

Address	Write Function	Read Function
D0000H	Write printer data register	Read printer data register
D0002H	Write configuration register	Read configuration register
D0004H	no write function	Read interrupt register
D0006H	Write loopback configuration register	Read loopback configuration register

3.3.8.3 Data Write Cycle

The actual printer data is written one byte at a time. After a byte of data has been written to the data register, the microprocessor returns to perform other functions while waiting for a printer interrupt (microprocessor level 1 "option interrupt"). When the data is written to the data register, a delay strobe begins which will trigger the printer *DATA STROBE/*. The completion of the *DATA STROBE/* clocks the data into the printer. No further action takes place until the printer responds with an *ACKNLG*. The data acknowledge sets an *ACKNLG* flip-flop, and if the *ACKNLG* interrupt enable bit in the command register is set, an "option interrupt" occurs, completing the data write cycle.

3.4 HPS-7088-030 INTERFACE

3.4.1 SLAVE INTERFACE AND BUFFER

The HPS-7088-030 consists of a master and a slave board. The master board buffers address and data busses for expansion to the slave board. Necessary control signals and the buffered address and data busses are connected to the slave board via a pair of multi-conductor ribbon cables.

3.4.2 SLAVE LOGIC

The slave logic functions similarly to that of the master board in the areas defined below:

- **RS-232C Interface:** The RS-232C interface logic is identical to that described in section 3.1.5.
- **Interrupt Circuit:** The interrupt circuit logic responds only to interrupt levels 6, 4, and 2 described in section 3.2.4.
- **Read and Write Cycles:** EPROM read and RAM write cycles are handled as described in sections 3.3.1 and 3.3.3, respectively.