#51

DEPOT INFORMATION BULLETIN | Field Service

HiCC

Subject: NOVA 1200 POWER UP AND POWER DOWN SEQUENCE.

Nova 1200 CPU Print (001-008-19)

POWER UP

When power is first turned on, the +5 O.K. line provides a positive transition (to approximately 4.4 volts) as the +5 volt output rises to its proper level. This positive transition is gated into a differentiating capacitor to produce a pulse which in turn drives the RESET and PRESET gates (1-B8) $\overline{\text{RESET}}$ and $\overline{\text{PRESET}}$ initializes the control logic of the CPU in preparation for operation.

After +5 comes up $\overline{\text{PWR FAIL}}$ goes from a low to a high causing AC CLR Flop to set and then reset. (1-A6) When AC CLR Flop sets $\overline{\text{LOAD AC}}$ goes low. (3-D3) As $\overline{\text{AC CLR}}$ goes low the output of the shifter produces all highs. (4-A8) $\overline{\text{AC CLR}}$ along with ACTG0 and ACTG1 cause a shift pulse to be produced on the IR register. (1-A8) When +5 volts reaches the IR register I 4, its outputs are high. $\overline{\text{IR3}}$ is gated back to U12 causing a low on the DS input of U30.

Since the SH input is high on U30, its outputs will be clocked down to zero and then to ones. The IR bits are changing which cause the ACC SEL lines to change also. All 4 accumulators have been selected with the ACS SEL and ACTG input lines. The ACD and ACS are loaded with zeros due to the inversion of the inputs.

Submitted by: EMILE BERTHELETTE	Date: 12/11/75
Reviewed by: David Hanna	Date: 12/11/75

POWER DOWN

$\overline{\text{PWR FAIL}}$ going low sets POWER LOW FLAG when line voltage drops to 90% of nominal voltage. (30D7) MEM OK resets the RUN flag and stops the computer when the +VMEM (+Vdc) voltage goes too low for the memory to function reliably.