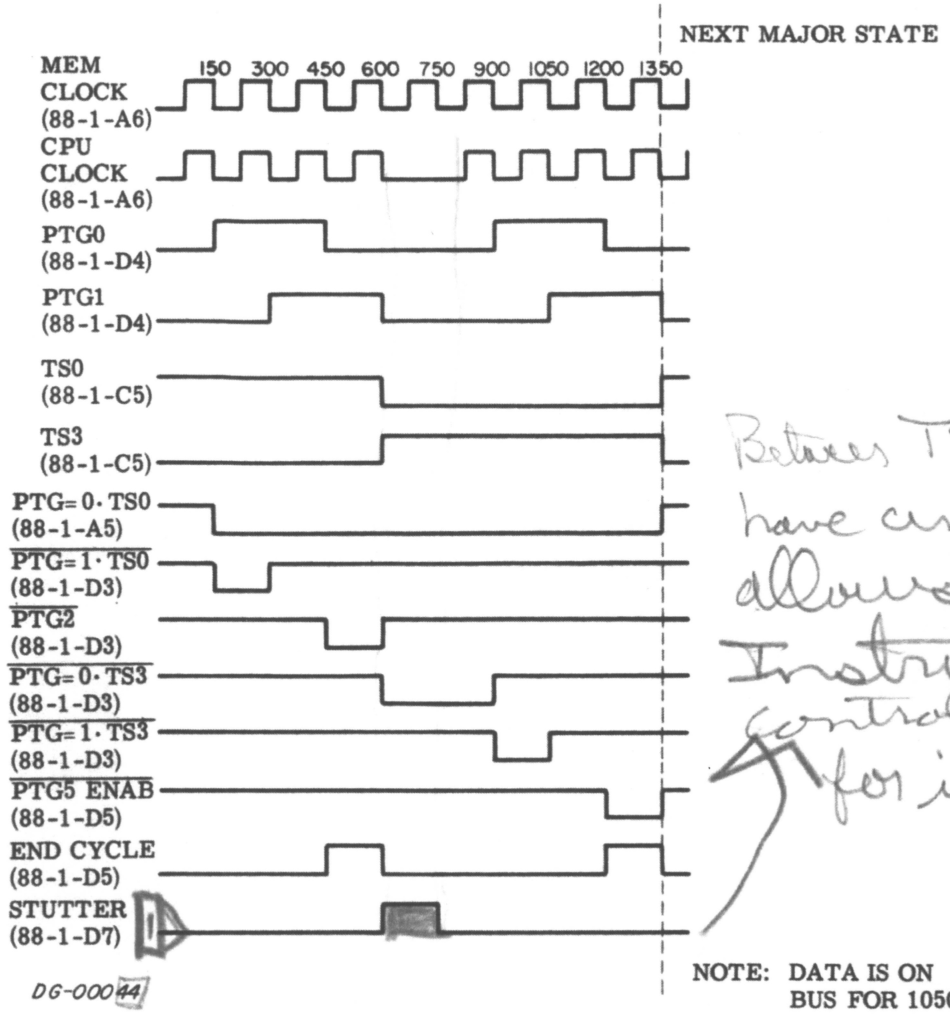

NOTE: DATA IS ON BUS FOR 1050μsec.

Figure C-2 Timing For The Processor Timing Generator During Fetch or Key

Between TS0 + TS3 have an extra 150 Ns allows time to decode Instruction and set up controls for ~~last~~ that are neccessary for instruction 1

Process Time
Accumulator Timing
Memory Timing Gen

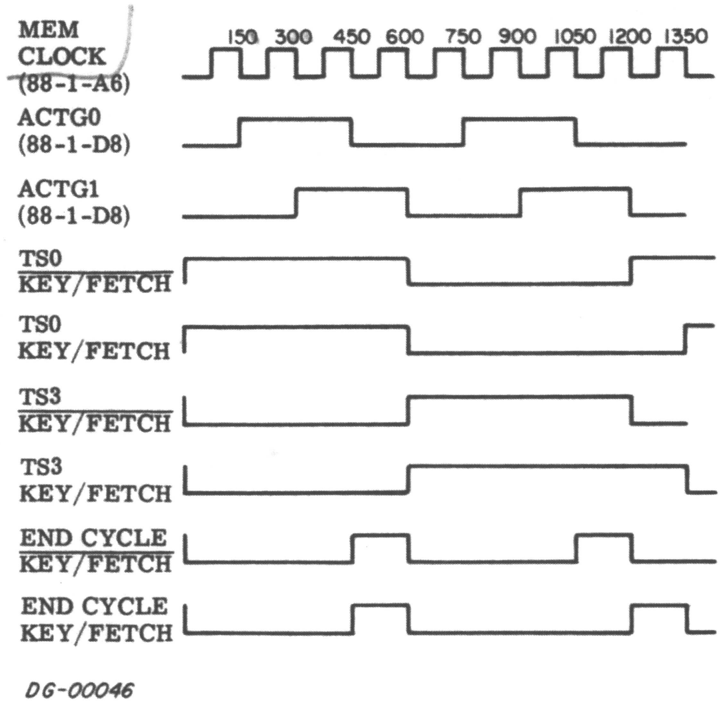

Figure C-3 Timing For The Accumulator Timing Generator

ACCUMULATOR TRUTH TABLE (88-4-B6 & B7 U124 & U123)