Model 990 SMD+

SMD Disk Controller

Technical Manual

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REVISION HISTORY

ECO No.	Date	Description	Pages
0328	6/28/85	New ZETACO Cover	
0459	5/15/85	Support of 931 by Diagnostic Tape	
0522	10/21/85	Addition of Alternate Track Mapping (Option)	
0523	3/4/86	New Cover	

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1.0 INTRODUCTION

The ZETACO, Inc. 990 Storage Module Disk Controller (990 SMD+) interfaces any Texas Instruments' 990, BS600 and BS800 Computer System that uses the high-speed TILINE* bus with most industry standard SMD Disk Drives and provides full emulation of standard DX10 and DNOS software.

1.1 FEATURES

- Interfaces to the high-speed TILINE bus and operates with standard "DX" software
- Simultaneous Control of up to (4) SMD Interface Disk Drives
- Full use of Drive capacities to over 600 Mb
- Mix Drives of differing types and capacities
- On-board 32 bit error checking and correcting of burst errors up to 11 bits in length
- High speed Microprocessor design supports maximum transfer rates
- On-board Self-Test with error reporting and LED display
- Diagnostic test program included with each controller
- Sector Interleaving
- Support Overlap Seeks
- Offset Positioning and Clocking for Data Error Recovery
- Alternate Track Mapping of Bad Tracks (Optional)
- Full 2-Year Warranty

*TILINE is a registered trademark of Texas Instruments, Inc.

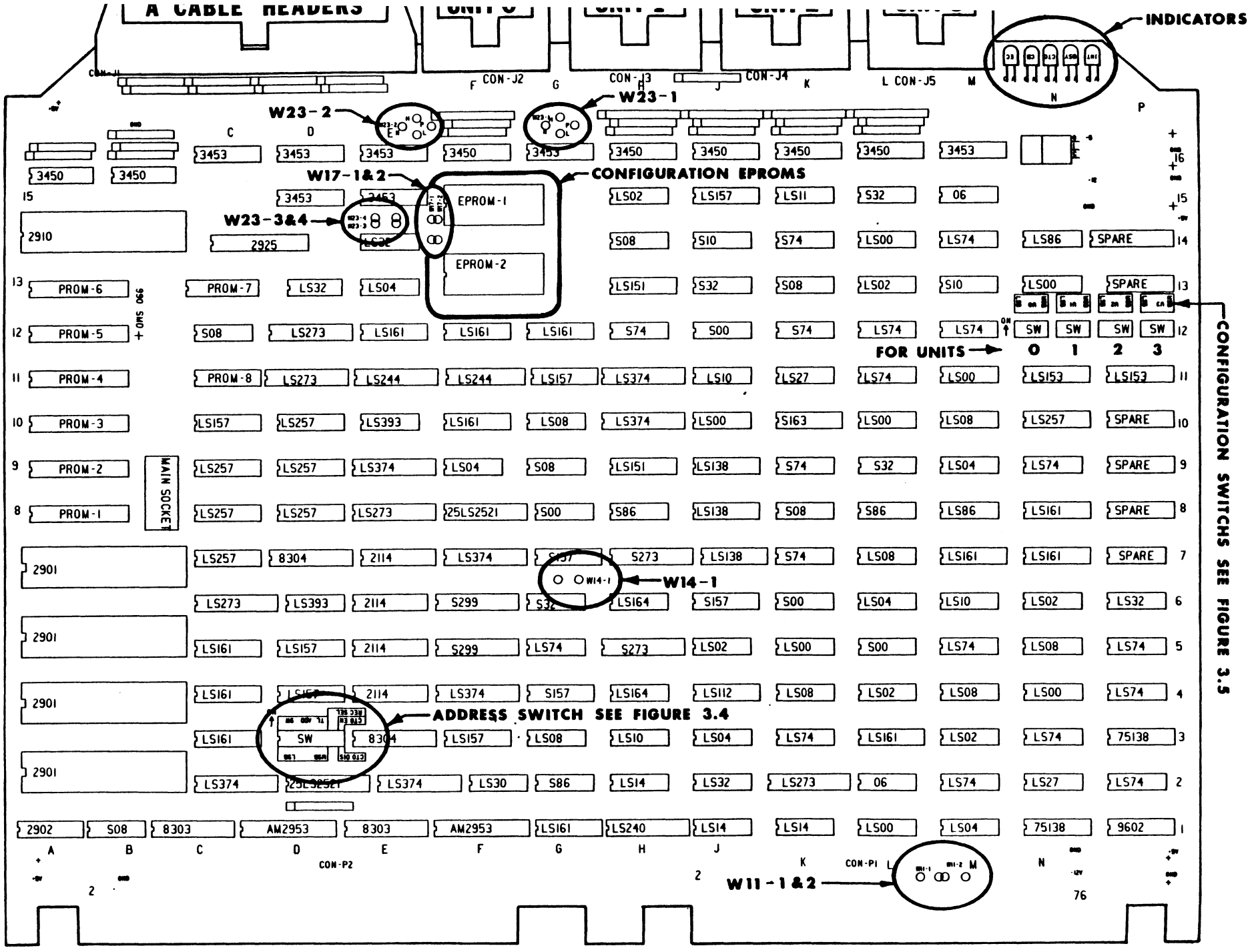


FIGURE 1.1 990 SMD PC. BOARD LAYOUT

2.0 SPECIFICATIONS

2.1 INTERFACE

The Interface to the computer system is the Texas Instruments high-speed TILINE Bus.

The Drive Interface is the industry standard SMD Interface with differential Drivers/Receivers. Up to four drives per controller (CMD and LMD counts as two each). Cabling is done with two cables per drive, a 26 Pin Ribbon Cable ("B" Cable) from each drive to the controller and a 60 Pin Ribbon Cable ("A" Cable) is daisy chained from the controller to each drive in turn, with a terminator on the last drive.

2.2 POWER

+5 VDC @ 6.1 Amps nom.
-12 VDC @ 0.5 Amps nom.

2.3 PHYSICAL

Dimensions:

361.95 millimeters (14.25 inches) by 274.32 millimeters (10.8 inches) by 12.7 millimeters (0.5 inches)

Shipping Weight:

4.54 kg. - weight (10 pounds)
Includes cables, diagnostics and documentation

2.4 ENVIRONMENTAL

Operating Temperature: 0 to 55 C

Relative Humidity: 10% to 90% (non-condensing)

3.0 INSTALLATION

In order to install the 990 SMD+ Controller into the 990 computer system the controller, the system and the disk drive must be properly prepared.

To prepare the system refer to Section 3.2.

To prepare the controller refer to Section 3.3.

To prepare the disk drive refer to Section 3.4

The TILINE address, interrupt level and a slot in the chassis should be selected per the T.I. standard for disk subsystems. The standard selection for the primary disk controller is: TILINE address 0F800 Hex, interrupt level 13, chassis slot 7.

3.1 UNPACKING AND INSPECTION

On receipt of the 990 SMD+ from the carrier the shipping carton should have been inspected for any evidence of damage or mishandling in transit. However, before installing the controller it should be re-inspected.

If the product has signs of damage then contact the carrier and shipper immediately, specify the nature and extent of the damage and if the carton is un-opened then request that the carrier's agent be present when the carton is opened. However, this technical manual was inside of the carton and in that case it is already opened so keep the opened carton with the controller.

ZETACO's warranty does not cover shipping damage however, all controllers shipped by ZETACO, Inc. are insured and care should be taken by the user to preserve all evidence of shipping damage.

For repair or replacement of any ZETACO product damaged in shipment, call ZETACO to obtain Return Material Authorization instructions.

All parts comprising the Model 990 SMD+ are shipped in one container consisting of:

.990 SMD+ Controller

.Technical Manual

.Controller to Drive Cabling (optional)

.Diagnostic Software

The optional controller to drive cabling is for one disk drive and is fifteen feet long. The diagnostic software is on 1600 BPI 1/2 inch tape. Other configurations are available.

3.2 990 SYSTEM PREPARATION

For best results when changing the T.I. Model 990 system configuration use only the configurations recommended by T.I. for disk subsystems.

If the 990 SMD+ controller is to have the primary system disk on it then it should be configured for TILINE address 0F800 Hex, interrupt level 13 and use chassis slot 7. If it is the secondary disk controller then refer to your T.I. supplied "Hardware User's Guide" and/or the "DX10 Operating System - Systems Programming Guide, Volume V" for other configurations.

When a system configuration is selected then the DX10 operating system must have all disk drives gened into it. If no new disk drives need to be added (all drives, DS01--DSXX, are already generated into the system) then all that needs to be done is to prepare the chassis slot (see Section 3.2.1) or else refer to your T.I. supplied "DX10 Operating System - Systems Programming Guide, Volume V" to generate a new system with the new drive added.

The selected TILINE address and interrupt level must not be assigned to any other device in the system.

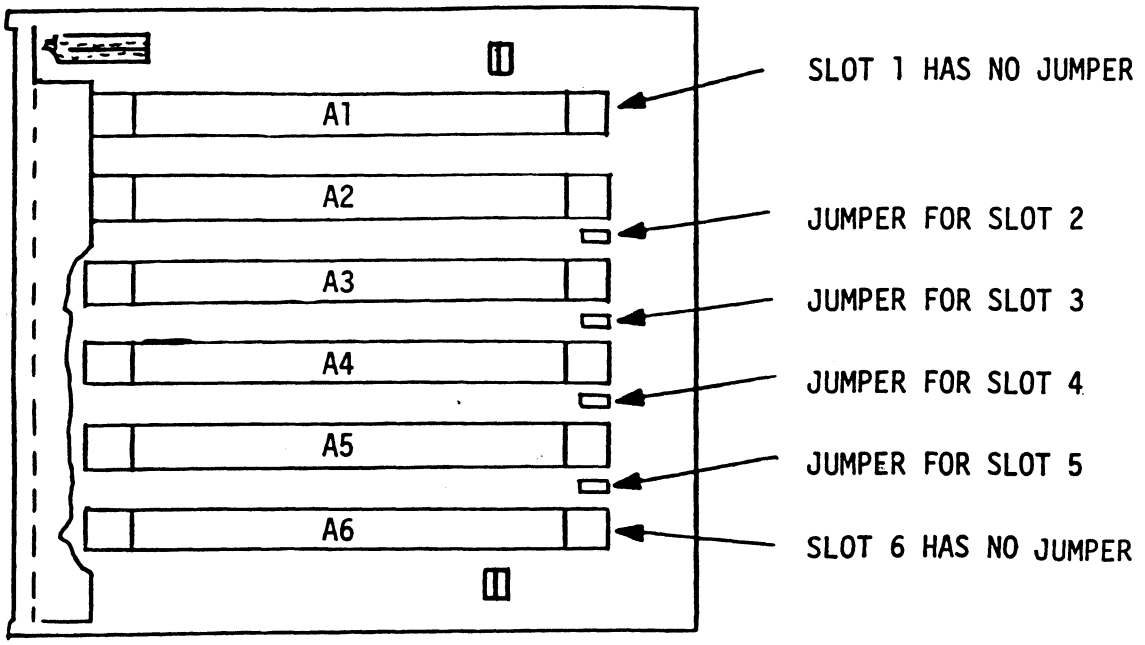
To make use of the optional alternate track feature, the drive type table in the IDS Program will need to be patched, see Section 3.2.2.

3.2.1 CHASSIS SLOT PREPARATION

The 990 SMD+ Controller occupies one full TILINE slot.

Most slots in the 990 Chassis have a jumper called the "Access Granted" jumper. The slot chosen for the 990 SMD+ must have this jumper opened (or removed) before installing the board. Some chassis require that wires be cut, or that a switch be opened. Refer to your T.I. supplied "Hardware User's Guide" for additional information. Figures 3.1, 3.2 and 3.3 depicts 6, 13, 17-slot chassis access jumpers or switches.

The selected interrupt level should be on the P2 side of the selected chassis slot. If it is not on the P2 side but it is on the P1 side then the 990 SMD+ controller may be re-configured with the interrupt on the P1 side (refer to Section 3.3.2).

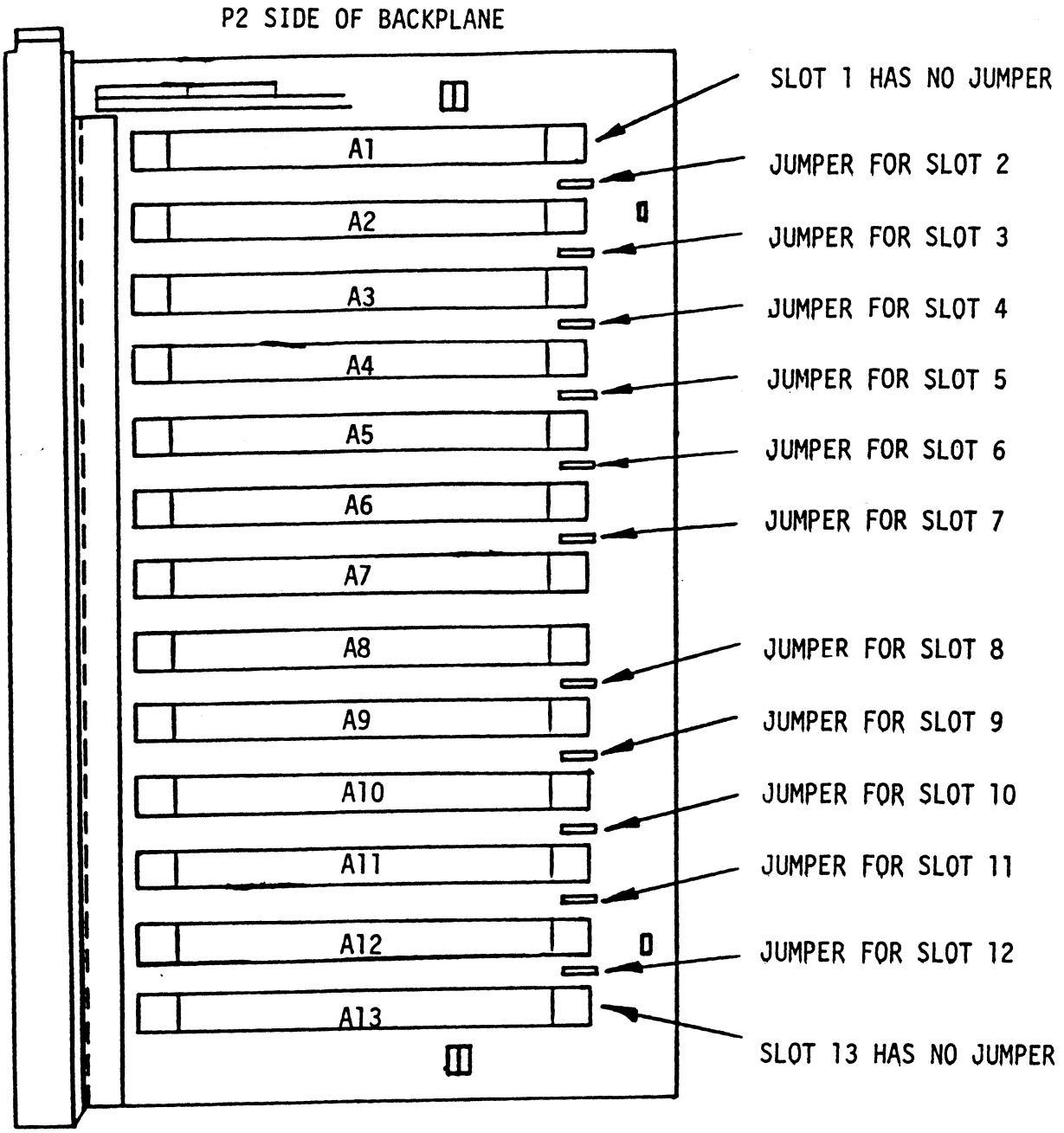


NOTE

JUMPERS ARE REMOVABLE JUMPER PLUGS.

THE JUMPER MUST BE REMOVED FROM THE SLOT THAT THE 990 SMD+ IS TO GO INTO.

FIGURE 3.1 SIX-SLOT CHASSIS, ACCESS JUMPERS

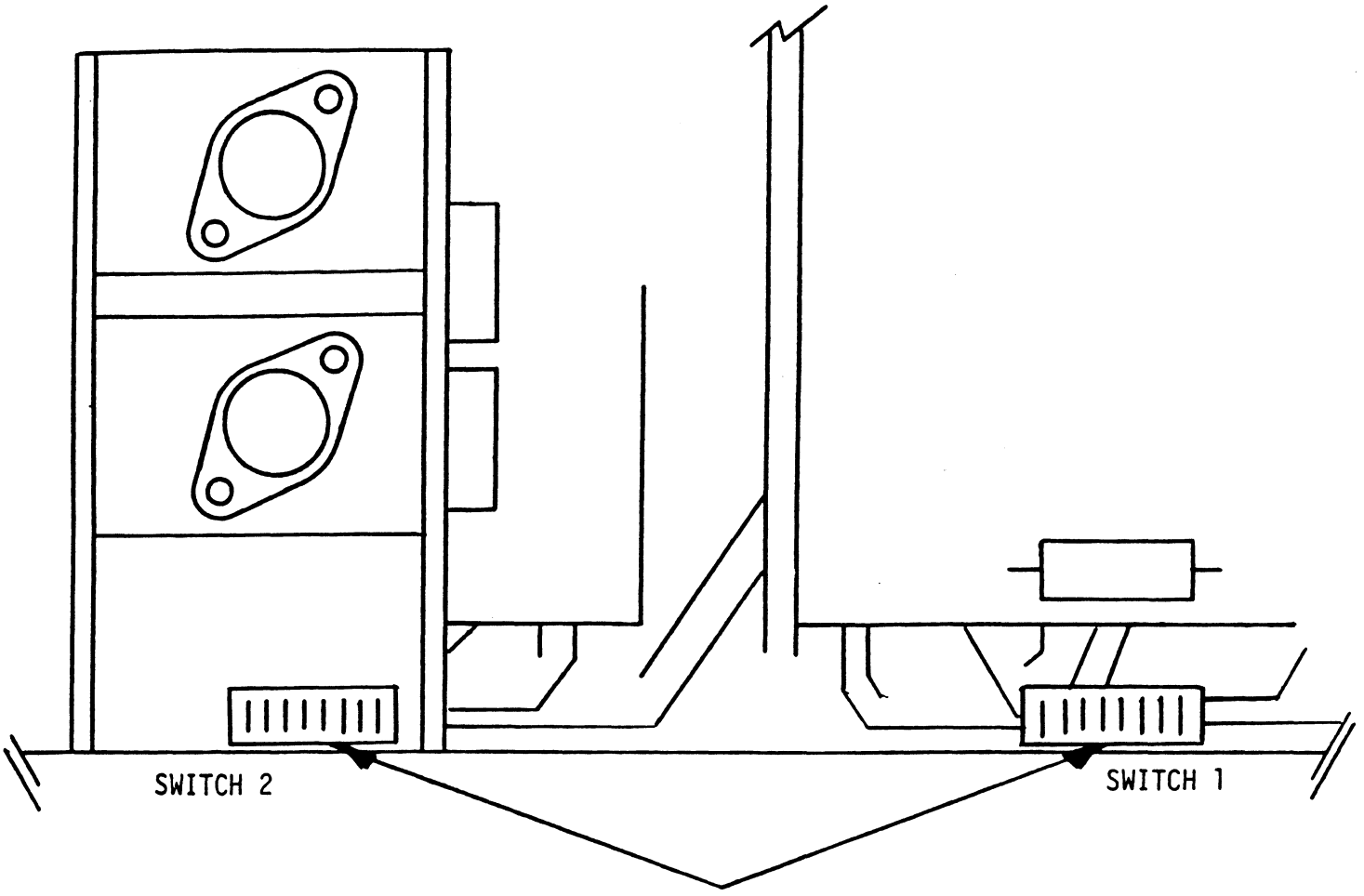


NOTE

JUMPERS ARE REMOVABLE JUMPER PLUGS.

THE JUMPER MUST BE REMOVED FROM THE SLOT THAT THE 990 SMD+ IS TO GO INTO.

FIGURE 3.2 THIRTEEN-SLOT CHASSIS, ACCESS JUMPERS



NOTE

SLOTS 1 AND 17 HAVE NO JUMPER.

THE SWITCH MUST BE SET TO OFF FOR
THE SLOT THAT THE 990 SMD+ IS TO GO INTO.

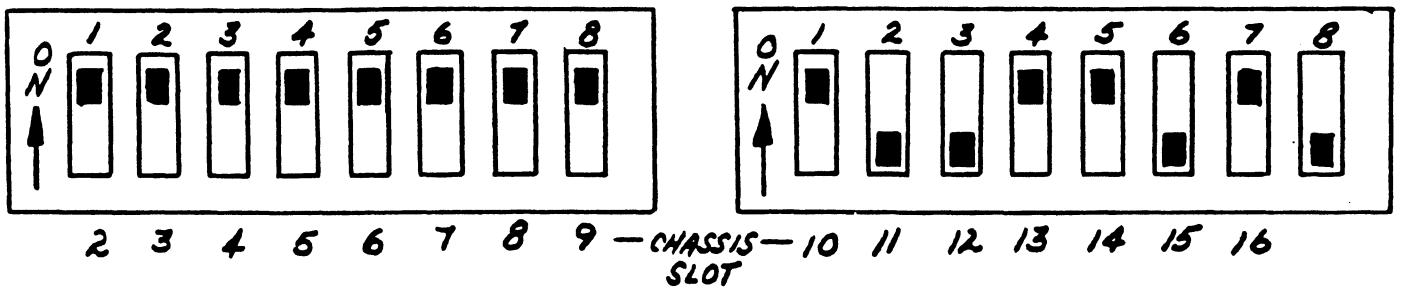


FIGURE 3.3 SEVENTEEN-SLOT CHASSIS, ACCESS JUMPERS

If the selected interrupt level is not on the P2 or P1 side of the selected chassis slot then the chassis interrupt configuration may need to be changed or else a new level or slot need to be selected. Refer to your T.I. supplied "Hardware User's Guide" when attempting to modify system interrupts. However, not all chassis can have the interrupts re-configured and then the interrupt level or slot will need to be re-selected, see Section 3.2.

3.2.2 ALTERNATE TRACK MAPPING (OPTION)

The ability to do alternate track mapping is available as an option on the 990 SMD+ Disk Controller.

The drive type table in the IDS Program will need to be patched. The patch is to turn on alternate track mapping, transfer, inhibit and set up the number of mapping cylinders. The patch will need to be made to the unknown drive or to a new drive added to the table for the selected disk.

NOTE: THE USER MUST PATCH THE IDS PROGRAM IN ORDER TO USE ALTERNATE TRACK MAPPING.

3.3 990 SMD+ CONTROLLER PREPARATION

To prepare the 990 SMD+ controller for use, the following will need to be done:

-Set up the TILINE address switches to the selected address.

-If the interrupt is to be on the P1 instead of the P2 side of the chassis then the interrupt jumpers will need to be changed.

-Set up the four configuration switches per the selected disk drives to be used.

3.3.1 TILINE ADDRESS SWITCH PREPARATION

The TILINE address that was selected in Section 3.2 needs to be set up on the 990 SMD+ controller. This address is the base address of the eight control words (see Section 4.0) that is used to transfer commands and status between the system and the 990 SMD+. This address is set with six switches of an eight-bay dip switch. The dip switch is located at I.C. location D3, refer to Figure 1.1.

Figure 3.4 depicts the TILINE address switch bank and the corresponding TILINE address bits. Only the first six switches are used for the TILINE address. All possible address combinations and their corresponding switch settings are listed in Table 3.1.

T.I.'s standard base address for the primary disk controller is 0F800 Hex, for this address all six switches would be on.

NOTE

This Eight-Bay Dip Switch is located at Board Location D3.

The Switches are set for TILINE Address 0F800 Hex and Command Time-Out Enabled

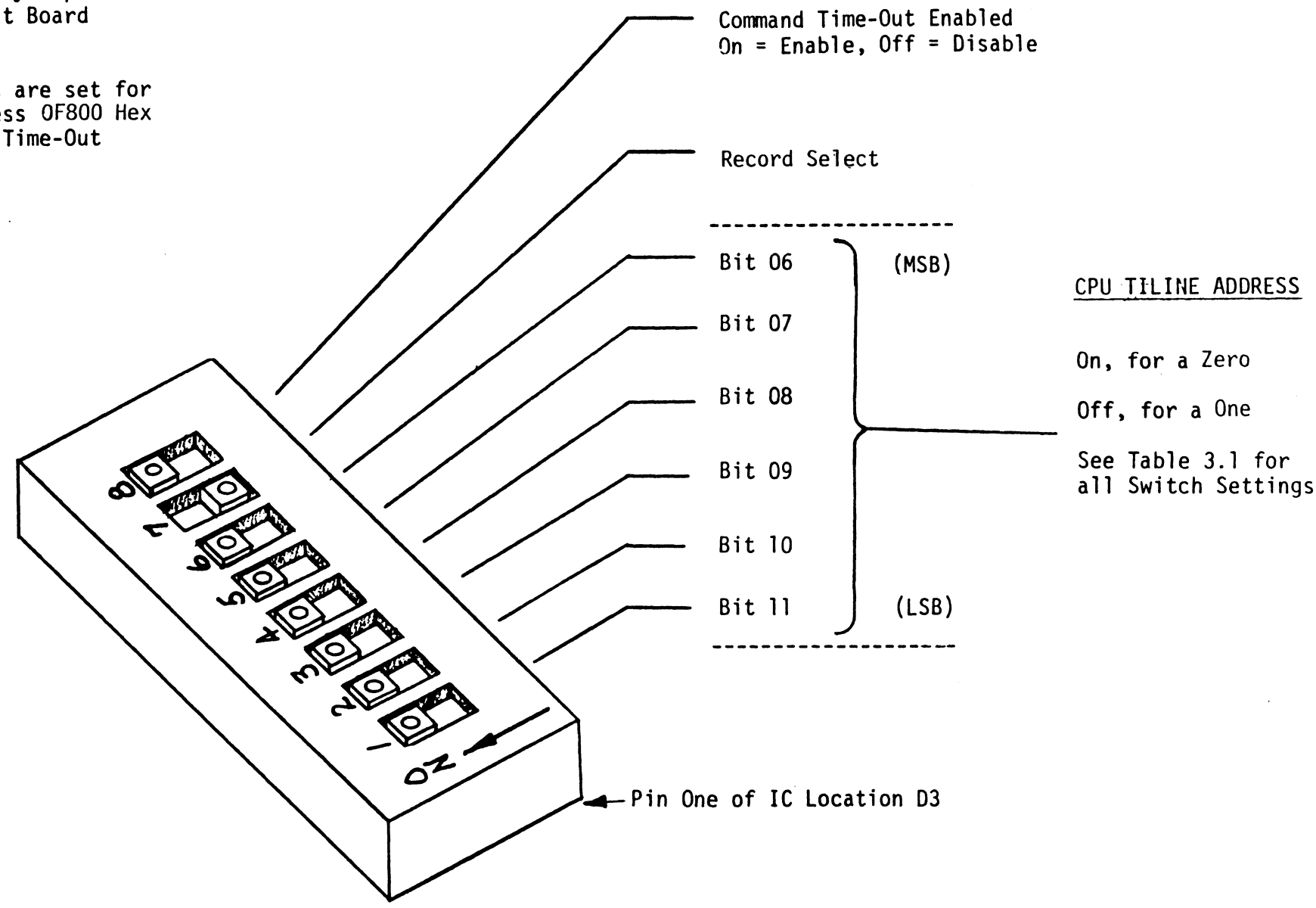


FIGURE 3.4 ADDRESS SWITCH

CPU BYTE ADDRESS IN HEX	TILINE WORD ADDRESS IN HEX	SETTINGS FOR THE ADDRESS SWITCH ON = ZERO, OFF = ONE *					
		MSB SW6	SW5	SW4	SW3	SW2	LSB SW1
F800	FFC00	ON	ON	ON	ON	ON	ON
F810	FFC08	ON	ON	ON	ON	ON	OFF
F820	FFC10	ON	ON	ON	ON	OFF	ON
F830	FFC18	ON	ON	ON	ON	OFF	OFF
F840	FFC20	ON	ON	ON	OFF	ON	ON
F850	FFC28	ON	ON	ON	OFF	ON	OFF
F860	FFC30	ON	ON	ON	OFF	OFF	ON
F870	FFC38	ON	ON	ON	OFF	OFF	OFF
F880	FFC40	ON	ON	OFF	ON	ON	ON
F890	FFC48	ON	ON	OFF	ON	ON	OFF
F8A0	FFC50	ON	ON	OFF	ON	OFF	ON
F8B0	FFC58	ON	ON	OFF	ON	OFF	OFF
F8C0	FFC60	ON	ON	OFF	OFF	ON	ON
F8D0	FFC68	ON	ON	OFF	OFF	ON	OFF
F8E0	FFC70	ON	ON	OFF	OFF	OFF	ON
F8F0	FFC78	ON	ON	OFF	OFF	OFF	OFF
F900	FFC80	ON	OFF	ON	ON	ON	ON
F910	FFC88	ON	OFF	ON	ON	ON	OFF
F920	FFC90	ON	OFF	ON	ON	OFF	ON
F930	FFC98	ON	OFF	ON	ON	OFF	OFF
F940	FFCA0	ON	OFF	ON	OFF	ON	ON
F950	FFCA8	ON	OFF	ON	OFF	ON	OFF
F960	FFCB0	ON	OFF	ON	OFF	OFF	ON
F970	FFCB8	ON	OFF	ON	OFF	OFF	OFF
F980	FFCC0	ON	OFF	OFF	ON	ON	ON
F990	FFCC8	ON	OFF	OFF	ON	ON	OFF
F9A0	FFCD0	ON	OFF	OFF	ON	OFF	ON
F9B0	FFCD8	ON	OFF	OFF	ON	OFF	OFF
F9C0	FFCE0	ON	OFF	OFF	OFF	ON	ON
F9D0	FFCE8	ON	OFF	OFF	OFF	ON	OFF
F9E0	FFCF0	ON	OFF	OFF	OFF	OFF	ON
F9F0	FFCF8	ON	OFF	OFF	OFF	OFF	OFF

BOARD ADDRESS SWITCH SETTINGS

TABLE 3.1

CPU BYTE ADDRESS IN HEX	TILINE WORD ADDRESS IN HEX	SETTINGS FOR THE ADDRESS SWITCH ON = ZERO, OFF = ONE * MSB SW6	SW5	SW4	SW3	SW2	LSB SW1
FA00	FFD00	OFF	ON	ON	ON	ON	ON
FA10	FFD08	OFF	ON	ON	ON	ON	OFF
FA20	FFD10	OFF	ON	ON	ON	OFF	ON
FA30	FFD18	OFF	ON	ON	ON	OFF	OFF
FA40	FFD20	OFF	ON	ON	OFF	ON	ON
FA50	FFD28	OFF	ON	ON	OFF	ON	OFF
FA60	FFD30	OFF	ON	ON	OFF	OFF	ON
FA70	FFD38	OFF	ON	ON	OFF	OFF	OFF
FA80	FFD40	OFF	ON	OFF	ON	ON	ON
FA90	FFD48	OFF	ON	OFF	ON	ON	OFF
FAA0	FFD50	OFF	ON	OFF	ON	OFF	ON
FAB0	FFD58	OFF	ON	OFF	ON	OFF	OFF
FAC0	FFD60	OFF	ON	OFF	OFF	ON	ON
FAD0	FFD68	OFF	ON	OFF	OFF	ON	OFF
FAE0	FFD70	OFF	ON	OFF	OFF	OFF	ON
FAF0	FFD78	OFF	ON	OFF	OFF	OFF	OFF
FB00	FFD80	OFF	OFF	ON	ON	ON	ON
FB10	FFD88	OFF	OFF	ON	ON	ON	OFF
FB20	FFD90	OFF	OFF	ON	ON	OFF	ON
FB30	FFD98	OFF	OFF	ON	ON	OFF	OFF
FB40	FFDA0	OFF	OFF	ON	OFF	ON	ON
FB50	FFDA8	OFF	OFF	ON	OFF	ON	OFF
FB60	FFDB0	OFF	OFF	ON	OFF	OFF	ON
FB70	FFDB8	OFF	OFF	ON	OFF	OFF	OFF
FB80	FFDC0	OFF	OFF	OFF	ON	ON	ON
FB90	FFDC8	OFF	OFF	OFF	ON	ON	OFF
FBA0	FFDD0	OFF	OFF	OFF	ON	OFF	ON
FBB0	FFDD8	OFF	OFF	OFF	ON	OFF	OFF
FBC0	FFDE0	OFF	OFF	OFF	OFF	ON	ON
FBD0	FFDE8	OFF	OFF	OFF	OFF	ON	OFF
FBE0	FFDF0	OFF	OFF	OFF	OFF	OFF	ON
FBF0	FFDF8	OFF	OFF	OFF	OFF	OFF	OFF

*See Figure 3.4

BOARD ADDRESS SWITCH SETTINGS

TABLE 3.1

3.3.2 ALTERNATIVE INTERRUPT SELECTION

If the interrupt is to be on the P1 side of the controller instead of the P2 side (refer to Section 3.2.1) then two jumpers on the 990 SMD+ will need to be changed. Jumper W11-1 is for the P1 connector and jumper W11-2 is for the P2 connector.

For the interrupt to be on the P1 connector then jumper W11-1 should be closed and jumper W11-2 should be open.

For the interrupt to be on the P2 connector then jumper W11-2 should be closed and jumper W11-1 should be open.

Refer to Section 9.3.1 for information on how to open or close jumpers.

3.3.3 CONFIGURING THE 990 SMD+ CONTROLLER

The 990 SMD+ will control up to four logical disk Units at a time (Unit 0 through Unit 3) that may be of differing types and capacities. For each one of the four units there is a 4-Bay DIP Switch (the configuration DIP switches) that will select one of fifteen drive types for the corresponding unit.

TO CONFIGURE THE CONTROLLER:

First, fill out the worksheet in Section 8.0. The worksheet will help place drives at the proper unit address. Then it will help find the approriate configuration DIP switch settings.

Second, set up the configuration DIP switches for each unit per the worksheet. To locate the switches refer to Figure 1.1 and for a closer look refer to Figure 3.5.

3.3.3.1 THE TWO RECORD CONFIGURATION EPROMS

The controller may be equipped with two configuration records (Addendum 1 will indicate it if it is). To select one of them use the address switch (refer to Figures 1.1 and 3.4) bay seven (refer to Section 8.2), the switch is called RECORD SELECT.

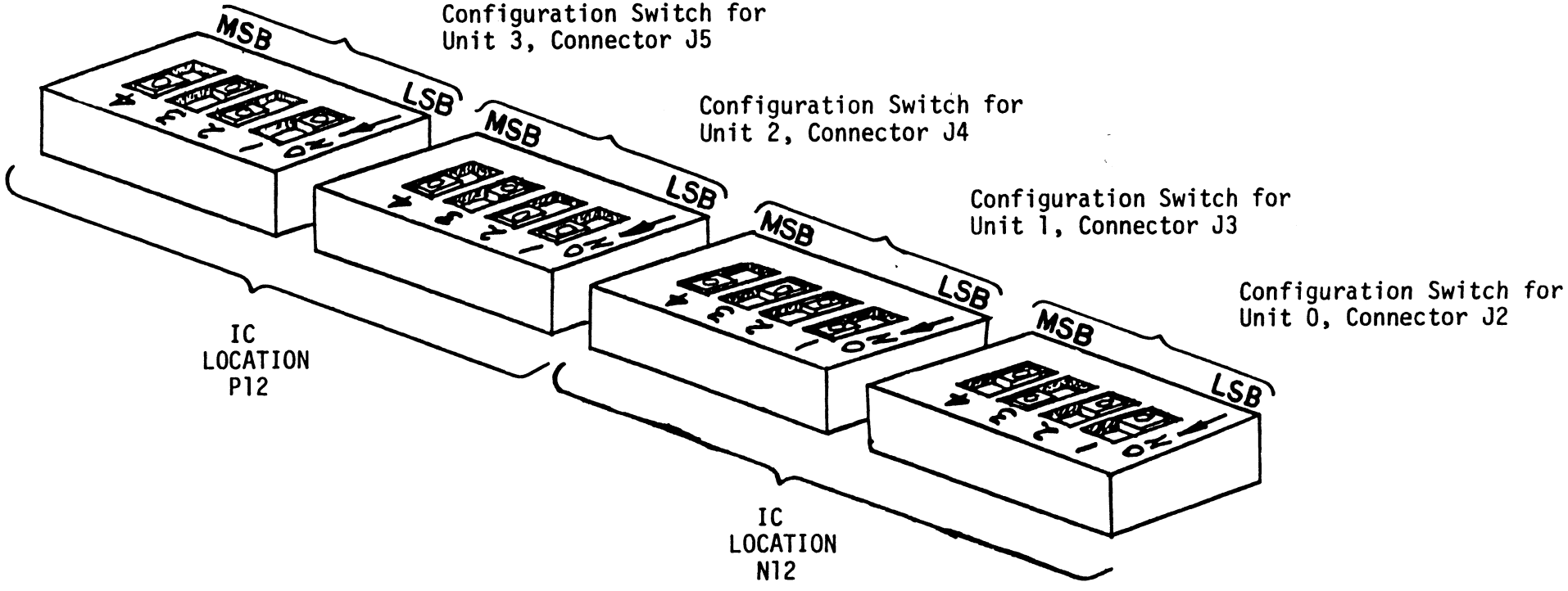
3.4 DISK DRIVE PREPARATION

It is beyond the scope of this manual to show all the switch settings of all the drives thus, the user must refer to the disk drive documentation.

NOTE

The Four, Four-Bay, Dip Switches are set per Unit to the following:

	BANK	SW4	SW3	SW2	SW1
UNIT 0 =	11	OFF	ON	OFF	OFF
UNIT 1 =	6	ON	OFF	OFF	ON
UNIT 2 =	4	ON	OFF	ON	ON
UNIT 3 =	5	ON	OFF	ON	OFF



See Table 3.2 for all Switch Settings

FIGURE 3.5 CONFIGURATION SWITCHES

THE EPROM BANK SELECTED	SETTINGS OF THE CONFIGURATION SWITCH ON = ZERO, OFF = ONE *			
	MSB SW4	SW3	SW2	LSB SW1
0	ON	ON	ON	ON
1	ON	ON	ON	OFF
2	ON	ON	OFF	ON
3	ON	ON	OFF	OFF
4	ON	OFF	ON	ON
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	ON
7	ON	OFF	OFF	OFF
8	OFF	ON	ON	ON
9	OFF	ON	ON	OFF
10	OFF	ON	OFF	ON
11	OFF	ON	OFF	OFF
12	OFF	OFF	ON	ON
13	OFF	OFF	ON	OFF
14	OFF	OFF	OFF	ON
15	OFF	OFF	OFF	OFF

NOTES:

* See Figure 3.5

Each one of the Four, Four-Bay Dip Switches will select the EPROM Bank for the corresponding Unit. One Four-Bay Dip Switch per Disk Unit.

CONFIGURATION SWITCH SETTINGS

TABLE 3.2

The unit address and the sectors per track will need to be set up in the drive. Refer to the worksheet in Section 8.0 for the disk drive unit address and the sector setting. A multiple volume drive will need to be set to the lower unit address. Refer to the Worksheet in Section 8.0. (Multiple volume drives are not available with Alternate Track Mapping.)

3.5 INSERTING THE BOARD INTO THE CHASSIS

With system power turned off insert the board (component-side to the same side as the other boards in the chassis) into the selected slot, with the disk cable headers away from the backplane. Apply slight pressure to the card ejectors (not the board's front edge or connectors.... damage may result) until the board is firmly seated into the computer's backplane connectors.

3.6 CABLING

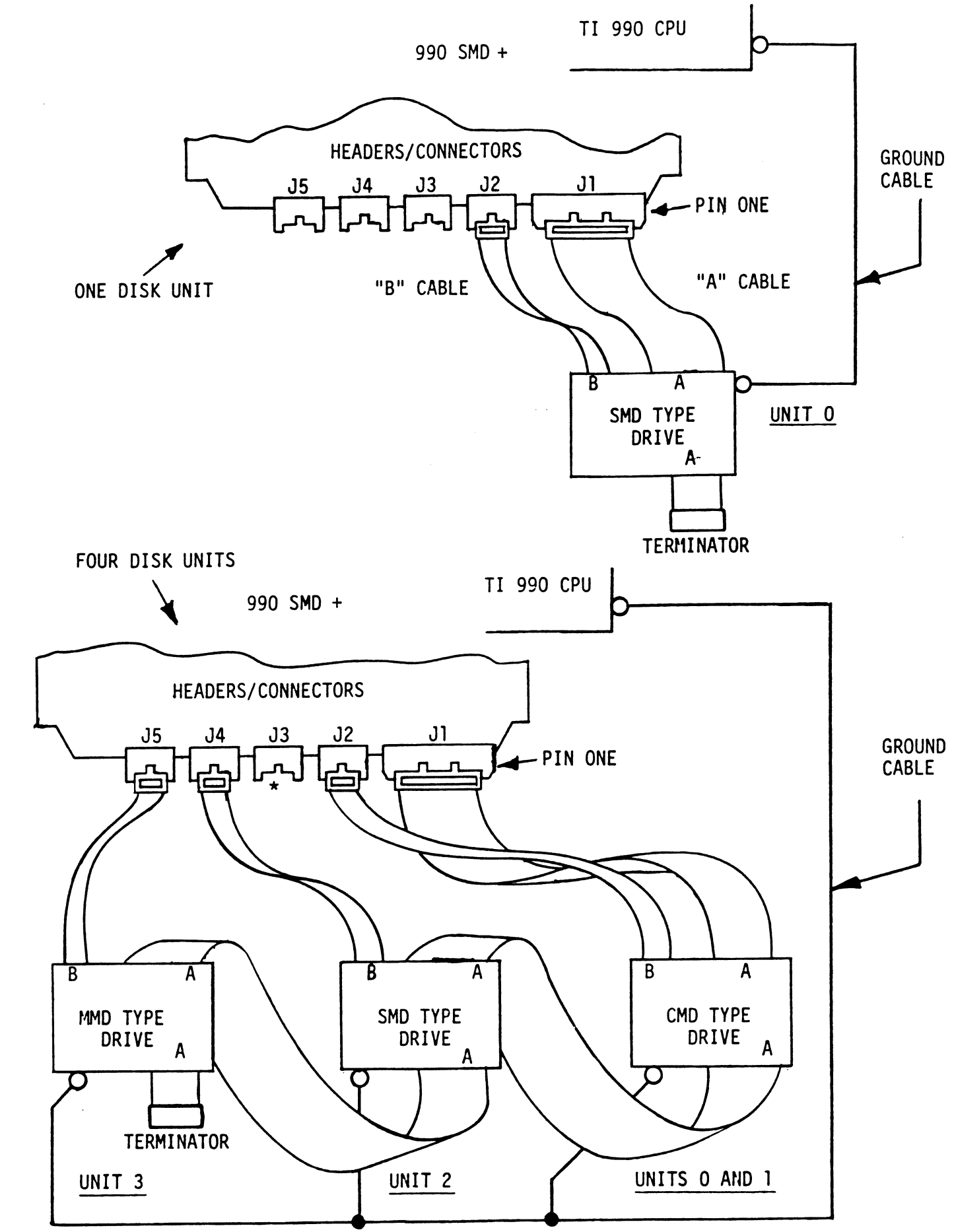
Reference Figure 3.6 for proper cable connection and Figure 1.1 for Header Locations and orientations. Be sure to observe the arrows on the Headers and Plugs for proper orientations.

As shown in Figure 3.6 the 60 Pin Cable (the A Cable) connects between J1 and the first drive. Then as more drives are added a new A Cable will go from the last drive to the new one. The A Cable continues through drive after drive in a daisy chain fashion up to the last drive in the chain and that drive must have a terminator installed in place of the missing cable.

Each drive must have a 26 Pin Cable (the B Cable) connecting the controller with each drive in a radial fashion. Unit 0 through Unit 3 will use Header J2 through J5 respectively.

The drive type selected for each Header must correspond to the drive type plugged into its Header.

A multiple volume drive will use two B Cable Headers (two units) but only one B Cable. The B Cable will go from the drive to the B Cable Header for the lower unit address. Refer to Worksheet in Section 8.0.



CMD Type Drives use two "B" Cable Headers

FIGURE 3.6 DISK CABLE CONNECTIONS

3.6.1 SYSTEM GROUNDING

Because the power system safety ground does not necessarily satisfy all system grounding requirements, additional connections are required to earth ground, referred to as system ground. The controller and its attached drive(s) must be connected to a single-point ground system. Ground connections are made via ground braids that pass from drive to drive, drive to computer chassis and computer chassis to earth ground.

WARNING: To ensure proper ground return to earth, each component in the system must be connected using a daisy chain ground system. Both the AC and DC grounds within each drive must be joined (consult drive manual). The drives must then be joined by a daisy chain grounding braid and connected to the grounding post at the rear of the computer cabinet.

3.7 POWERING-UP

Turn system power on. The 990 SMD+ will perform an initial Self-test. A "good" test is indicated by all LEDS being off and if not then refer to Sections 5.0 and 12.0 for diagnostic and trouble-shooting procedures.

It is recommended that the ZETACO Reliability be run to verify a working sub-system. Refer to Section 7.0.

4.0 PROGRAMMING THE CONTROLLER

The CPU uses eight consecutive words of TILINE Memory space, from a selected Base Address (see Section 3.2) to communicate with the controller. These eight words, Control Word 0 (CW0) through Control Word 7 (CW7) (see Figure 4.1) contain the following information:

CONTROL WORD 0 (CW0)

CW0 contains the Real Time Disk Status of the selected disk drive, if one is selected. Plus the Attention and Attention-Mask Bits for generating an Attention Interrupt. Only the Attention-Mask Bits may be written by the CPU.

CONTROL WORD 1 (CW1)

CW1 contains the Disk Command Codes, the starting Head Address and Control Bits to assist in Data Recovery Operations.

CONTROL WORD 2 (CW2)

CW2 contains the Starting Sector Address and the number of sectors per record.

CONTROL WORD 3 (CW3)

CW3 contains the Starting Cylinder Address.

CONTROL WORD 4 (CW4)

CW4 contains the number of Bytes to be transferred between the CPU Memory and the Disk.

CONTROL WORD 5 (CW5)

CW5 contains the least significant bits of the TILINE Memory Address, the Address is a Byte Address.

CONTROL WORD 6 (CW6)

CW6 contains the most significant bits of the TILINE Memory Address, see CONTROL WORD 5 (CW5), and the drive select bits.

CONTROL WORD 7 (CW7)

CW7 contains the Controller Status Bits, the Interrupt Enable Bit and the Idle/Busy Bit. See Section 4.3 for more detailed information on the Control Words.

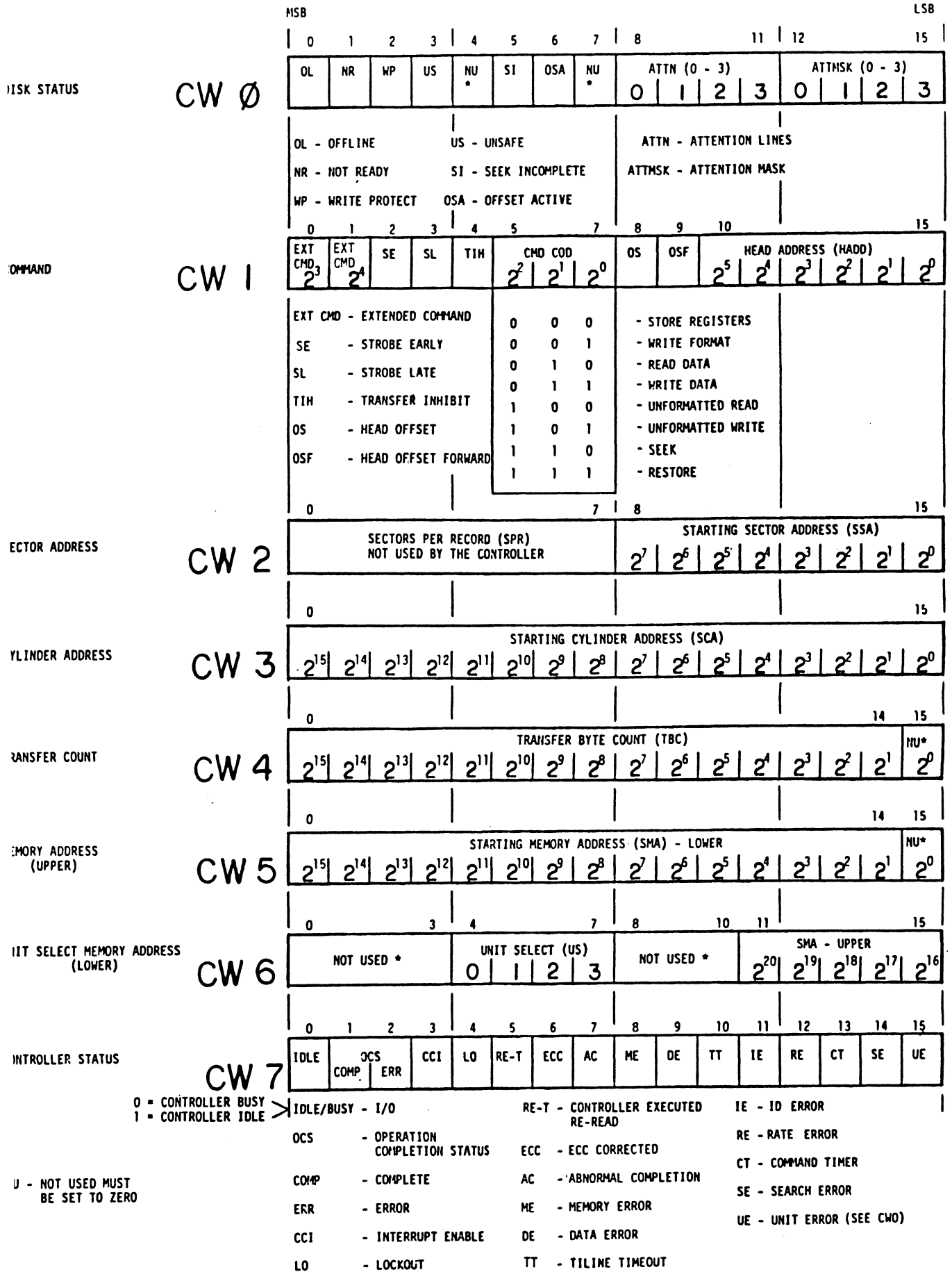


FIGURE 4.1 CONTROL WORD FORMAT

Controller operation is initiated by writing the desired Command and its associated parameters into the appropriate Control Words. The order in which the Control Words are written is not important except that CW7, Bit 0 must be written last. The controller will immediately begin execution of the operation specified by the Control Words as soon as CW7 is written with a word that has Bit 0, MSB, set to a zero. This puts the controller into the Busy Mode.

Any attempts by the CPU to write to a Busy controller will result in a NOP-WRITE. A NOP-WRITE will complete normally, except that the selected Control Word will not be written into.

Any attempts by the CPU to read any Control Word from a Busy controller will result in an EXTENDED STATUS READ. An Extended Status Read will pass four bits of information to the CPU. The Status Bits and their locations in the word read are:

Bit 0 Controller Idle/Busy, CW7 Bit 0 (MSB)

Bit 1 Control Slave Enable

Bit 2 Controller Bad

Bit 3 Error Code

Bit 4 through 15 are not used

See Section 5.0 for more information on these bits.

Before writing a Command to the controller Control Words, CW7 Bit 0 should first be checked to verify that the controller is Idle, CW7 Bit 0 is a One, and will accept the Command.

4.1 CONTROLLER COMMAND DESCRIPTIONS

The 990 SMD+ Controller upon receiving a Command from the CPU will perform any one of the twelve basic disk system Commands. If the controller has the Alternate Track Mapping option two more commands are available, Absolute Write Format and Relocate. These Commands are listed here for clarity only with the detailed command descriptions and examples deferred until later, in Section 4.4, for these descriptions require complete Control Word information, in Section 4.3.

STORE REGISTERS

A Store Registers Command causes the Disk Controller to return up to three words of disk sizing parameters to a specified TILINE Memory location.

WRITE FORMAT

A Write Format Command causes the disk controller to format a track on the selected disk unit. If the selected track has been relocated, the controller will seek to the alternate track and format that one instead.

ABSOLUTE WRITE FORMAT

An Absolute Write Format Command causes the controller to format a track. However, relocated tracks are ignored and alternate tracks are lost.

READ DATA

A Read Data Command will transfer data from a specified disk location to a specified TILINE Memory location. If the selected track has been relocated, the controller will seek to and get data from the alternate track.

WRITE DATA

A Write Data Command will transfer data from a specified TILINE Memory location to a specified disk location. If the selected track has been relocated, the controller will seek to and write data to the alternate track.

RELOCATE

A Relocate Command relocates a specified bad track to a specified spare track so that all disk operations to the relocated (bad) track are then performed on the alternate track.

Note that this command will format both tracks.

UNFORMATTED READ

An Unformatted Read Command causes the Disk Controller to return up to three words of Disk Format information to a specified TILINE Memory location.

EXTENDED UNFORMATTED READ

An Extended Unformatted Read Command will transfer a specified number of words from a specified Disk location, without regard to the Disk Format or existing record boundaries, to a specified TILINE Memory location.

UNFORMATTED WRITE

An Unformatted Write Command will transfer a specified number of words from a specified TILINE Memory location to a specified Disk location, without regard to the Disk Format or existing record boundaries.

SEEK

A Seek Command will position the heads to a specified cylinder address.

RESTORE

A Restore Command will clear certain disk errors and reposition the heads of the selected disk drive to cylinder zero.

T.I. SELF-TEST

The T.I. Self-test Command will cause the Disk Controller to do no disk operation but just return to the CPU that the controller is ready to go or no go.

ECC ON/OFF

An ECC On/Off Command will Enable or Disable the ECC correction function of the Controller.

RE-TRY ON/OFF

A Re-Try On/Off Command will Enable or Disable the Re-Try function of the controller.

4.2 COMMAND COMPLETION

When the controller has completed an operation it will enter the Idle Mode. Upon entering the Idle Mode an interrupt will be sent to the CPU if interrupts are enabled on the controller. Upon error-free completion of a Command the complete bit in CW7 will set. If the Command is not error-free then the error bit in CW7 will be set.

4.2.1 COMMAND COMPLETION INTERRUPT

The upper four bits in CW7 (Idle, Complete, Error and Interrupt Enable) control the Command Completion Interrupt. If this interrupt is to be on then bits Idle and Interrupt Enable must be on (set to a one) and complete or error bits on (set to a one).

4.2.2 ATTENTION INTERRUPT

The lower eight bits of CW0 control the Attention Interrupt. If one of the Attention Mask Bits is on (set to a one) and the corresponding Attention Bits are on and the controller is in the Idle Mode, then an interrupt will be sent to the CPU.

4.3 FORMAT AND USE OF THE CONTROL WORDS

For most of the controller operations the Control Words have fixed definitions with all exceptions noted in the detailed Command Descriptions Section 4.4.

See Figure 4.1 for the Control Word Format.

4.3.1 CONTROL WORD 0 (CW0)

CW0 is the disk drive Unit Status Word and the Attention Interrupt Enable Mask.

Bits 0 through 7 contains individual status indicators for the selected Unit. Bits 8 through 11 contain the Attention Line Status of each Drive Unit regardless of the drive selected. Bits 12 through 15 contain the Attention Mask Bits that are used with the Attention Bits to generate an interrupt. Each bit is defined as follows.

4.3.1.1 OFFLINE (OL) - CW0, BIT 0

Offline is set to indicate that the selected Unit is; 1) not powered up, 2) is not at the proper speed, 3) is not loaded with a cartridge, 4) that an unsafe condition exists, or 5) that no Unit is selected.

4.3.1.2 NOT READY (NR) - CW0, BIT 1

Not Ready is set when the selected Unit is offline, is performing a restore or seek operation, or that no Unit is selected.

4.3.1.3 WRITE PROTECT (WP) - CW0, BIT 2

Write Protect is set when the status from the selected Unit indicates that the Unit is Write protected. When activated, the Write protect circuit inhibits the disk drive write logic and neither format information nor data can be written on the disk.

4.3.1.4 UNSAFE (US) - CW0, BIT 3

Unsafe is set to indicate that an unsafe condition exists that prevents any disk operation, except a restore operation, from being executed, or that no Unit is selected.

4.3.1.5 CW0, BIT 4

Bit 4 of CW0 is not used and will be set to zero.

4.3.1.6 SEEK INCOMPLETE (SI) - CW0, BIT 5

The Seek Incomplete bit is set if the head carriage has failed to locate the specified cylinder. Some Seek Incomplete errors may be recovered from by performing a restore operation and then repeating the desired operation.

4.3.1.7 OFFSET ACTIVE (OSA) - CW0, BIT 6

The Offset Active bit is set to indicate that data was read from the disk using a head offset function in a disk read command.

4.3.1.8 CW0, BIT 7

Bit 7 of CW0 is not used and will be set to zero.

4.3.1.9 ATTENTION LINES (ATTN 0-3) - CW0, BITS 8 - 11

The position encoded Attention Bits reflect the Ready/ Busy (a one or zero respectively) status of each of the four disk units. If a unit does not have the heads into position to transfer data then that unit will be Busy, else it will be Ready. The heads may not be in a data transfer position just after a Seek or Restore Command.

CW0, BIT 8 = ATTENTION BIT 0 = UNIT 0

CW0, BIT 9 = ATTENTION BIT 1 = UNIT 1

CW0, BIT 10 = ATTENTION BIT 2 = UNIT 2

CW0, BIT 11 = ATTENTION BIT 3 = UNIT 3

4.3.1.10 ATTENTION MASK BITS (ATTNMSK 0-3) - CW0, BITS 12 - 15

The position encoded Attention Mask Bits control the Attention Interrupt. To enable or disable an Attention Interrupt for any of the four disk Units write a one or a zero (to enable or disable respectively) into the appropriate bits for the desired drive units. When the controller is in the Idle Mode, an Attention Line is ready, and the appropriate Attention Mask Bit is enabled then an Attention Interrupt will be sent to the CPU.

CW0, BIT 12 = ATTENTION MASK BIT 0 = UNIT 0

CW0, BIT 13 = ATTENTION MASK BIT 1 = UNIT 1

CW0, BIT 14 = ATTENTION MASK BIT 2 = UNIT 2

CW0, BIT 15 = ATTENTION MASK BIT 3 = UNIT 3

4.3.2 CONTROL WORD 1 (CW1)

CW1 contains the Command Code that specifies the desired controller operation and the head address. Bits 0 through 9 control requested operations; Bits 10 through 15 contains the surface address. This word is generally used only as a Control Word, however, the head address is incremented as disk operations are performed, and the head address at the end of an operation can be read for diagnostic purposes if desired. Bit functions are defined as follows.

4.3.2.1 EXTENDED COMMAND (EXT CMD) - CW1, BIT 0

The Extended Command bit is used with the three command code bits (CW1, Bits 5 - 7) to increase the number of possible command codes from 8 to 16. See Section 4.3.2.6.

4.3.2.2 CW1, BIT 1

Bit 1 of CW1 is not used and should be set to zero.

4.3.2.3 STROBE EARLY (SE) - CW1, BIT 2

This bit is used, when set to a one, to advance the Read Data Strobing in the disk drive in attempt to recover data that yields errors when read with normal strobe settings. Note that not all drives will have this function.

4.3.2.4 STROBE LATE (SL) - CW1, BIT 3

This bit is used, when set to a one, to retard the Read Data Strobing in the disk drive in an attempt to recover data that yields errors when read with normal strobe settings. Note that not all drives will have this function.

4.3.2.5 TRANSFER INHIBIT (TIH) - CW1, BIT 4

When Transfer Inhibit is set to a one no data will be written into the TILINE Memory until this bit is reset to a zero.

4.3.2.6 COMMAND CODES (CMD COD) - CW1, BITS 5 - 7

Table 4.1 lists the Command Codes and the Command Names. Detailed Command Descriptions and Examples are given in Section 4.4.

4.3.2.7 HEAD OFFSET (OS) - CW1, BIT 8

This bit is used, when set to a one, to enable the disk head offset positioning in an attempt to recover data that yields errors with heads in the normal position. Note that not all drives will have this function. See Section 4.3.2.8 for the offset direction.

4.3.2.8 HEAD OFFSET FORWARD (OSF) - CW1, BIT 9

If Bit 8 of CW1, see Section 4.3.2.7, has been set to a one then Bit 9 of CW1 will specify the direction of the offset. To Offset Forward set Bit 9 to a one and to Offset Backward set Bit 9 to a zero.

4.3.2.9 HEAD ADDRESS (HADD) - CW1, BITS 10 - 15

Bits 10 through 15 of CW1 select the head and associated platter surface, using a standard binary representation. Bit 15 is the LSB.

4.3.3 CONTROL WORD 2 (CW2)

CW2 contains the Starting Sector Address and sectors per record. Normally this word is used only for control, however, the Sector Address is updated during disk operations and can be read for diagnostic purposes. Bit functions are defined as follows.

4.3.3.1 SECTORS PER RECORD (SPR) - CW2, BITS 0 - 7

Since the Recording Format is always one sector per record, these bits are ignored by the controller.

4.3.3.2 STARTING SECTOR ADDRESS (SSA) - CW2, BITS 8 - 15

These bits select the Starting Sector Address for any disk data transfer, except Write Format.

4.3.4 CONTROL WORD 3 (CW3)

CW3 contains the Starting Cylinder Address. Normally this word is used only for control, however, the Cylinder Address is updated during disk operations and can be read for diagnostic purposes. Bit functions are defined as follows.

4.3.4.1 STARTING CYLINDER ADDRESS (SCA) - CW3, BITS 0 - 15

These bits select the Starting Cylinder Address for any operation, using a standard binary representation. Bit 15 is the LSB. At the start of a disk operation a Seek to the selected Cylinder Address is performed. An Invalid Address will result in a Seek Incomplete (SI), in CW0, Status from the disk and termination of the operation with Unit Error (UE), in CW7, set.

4.3.5 CONTROL WORD 4 (CW4)

CW4 contains the byte count for the transfer between the disk and the TILINE. Normally this word is used only for control however, the byte count is updated during disk operations and can be read for diagnostic purposes. Bit functions are defined as follows.

4.3.5.1 TRANSFER BYTE COUNT (TBC) - CW4, BITS 0 - 15

These bits, using a standard binary representation, selects the number of eight-bit data bytes that will be transferred between the disk and the TILINE. Bit 15, the LSB, must be zero, so that only even byte counts can be specified, because data is composed of two-byte words. The Byte Count Range is limited by available TILINE memory and the 64K-byte maximum specified in this Control Word. Any attempt to transfer to or from non-existent TILINE memory results in a TILINE Time-Out (TT) controller status, in CW7.

4.3.6 CONTROL WORD 5 (CW5)

CW5 contains the 16 least significant bits of the 21 bit TILINE Starting Address, with the five most significant bits in CW6. The TILINE Address is a Byte Address and data transfers is composed of two-byte words so Bit 15 of CW5 must be zero. Normally this word is used only for control, however, the TILINE Address is updated during disk operations and can be read for diagnostic purposes Bit functions are defined as follows.

4.3.6.1 STARTING MEMORY ADDRESS (SMA) - CW5, BITS 0-15: CW6, BITS 11-15

Bits 0 through 15 of CW5 and Bits 11 through 15 of CW6 make up the 21 Bit Starting Address for TILINE transfers. Using a standard binary representation the most significant five bits of the Address is in CW6 Bits 11 through 15, and the least significant 16 Bits is in CW5 Bits 0 through 15. CW5 Bit 15 must be set to zero, because data is composed of two-byte words. Any attempt to transfer to or from non-existent TILINE memory results in a TILINE Time-Out (TT) controller status, in CW7.

4.3.7 CONTROL WORD 6 (CW6)

CW6 contains the Unit Select Bits, in Bits 4 through 7, and the five most significant bits of the TILINE Address, in Bits 11 through 15. Normally this word is used only for control however, the TILINE Address is updated during disk operations and can be read for diagnostic purposes. Bit functions are defined as follows.

4.3.7.1 CW6, BITS 0 - 3

CW6, Bits 0 through 3 are not used and should be set to zero.

4.3.7.2 UNIT SELECT (US) - CW6, BITS 4 - 7

The position encoded Unit Select Bits select the drive unit desired for use in the next operation. To select a Unit set the appropriate Unit Select Bit to a one. Note that only one Unit Select Bit should be set at a time, and if no unit select bit is set then no unit will be selected. The unit select bit assignment is as follows.

CW6, BIT 4 = DRIVE UNIT 0 SELECT

CW6, BIT 5 = DRIVE UNIT 1 SELECT

CW6, BIT 6 = DRIVE UNIT 2 SELECT

CW6, BIT 7 = DRIVE UNIT 3 SELECT

4.3.7.3 CW6, BITS 8 - 10

CW6, Bits 8 through 10 are not used and should be set to zero.

4.3.7.4 STARTING MEMORY ADDRESS (SMA) - CW6, BITS 11-15: CW5, BITS 0-15

CW6, Bits 11 through 15 contain the five most significant bits of the Starting Memory Address. See Section 4.3.6 and 4.3.6.1 for more information on these bits.

4.3.8 CONTROL WORD 7 (CW7)

CW7 is the Controller Status and Control Word for all controller operations.

Bit 0, MSB, contains the Idle/Busy Status - Control Bit. Bits 1 and 2 contain the Operation Completion Status, error or no error. Bit 3 contains the Completion Interrupt Control Bit. Bit 4 contains a Control Bit for multiple CPU applications. Bits 5 and 6 contain Controller Error Re-Cover Status. Bits 7 through 15 contain the Controller Error Status Bits. Bit functions are defined as follows.

4.3.8.1 IDLE/BUSY (IDLE) - CW7, BIT 0

The controller must be in the Idle Mode, CW7 Bit 0 = One, for the processor to Read or Write the Control Words. The Idle/Busy Status may be read at any time. If the controller is Busy, CW7 Bit 0 = Zero, a Read of any Control Word, will give four bits of information, these bits are as follows:

BIT 0 = IDLE/BUSY, CW7 BIT 0 = ZERO (MSB)

BIT 1 = CONTROL SLAVE ENABLE

BIT 2 = CONTROLLER BAD

BIT 3 = ERROR CODE

See Section 5.0 for more information on these bits.

4.3.8.2 OPERATION COMPLETION STATUS (OCS) - CW7, BITS 1 AND 2

At the end of a command one of these Bits will be set by the controller and will reflect the Error Status of the command. If the command was error-free then the complete bit (Bit 1) will be set, to a one, else the error bit (Bit 2) will be set to a one.

The CPU may reset or set these bits as part of the Interrupt Service or Status Checking Routine, or may leave it alone until the next command is sent to the controller.

4.3.8.3 COMMAND COMPLETION INTERRUPT (CCI) - CW7, BIT 3

The Command Completion Interrupt Bit, CW7 Bit 3, is set to a one by the CPU to enable the controller to interrupt the CPU at the completion of a command. A Command Completion Interrupt occurs when the following logical condition is met:

IDLE and ((COMPLETE or ERROR) and COMMAND COMPLETION INTERRUPT)

Note that if the CCI Bit is set while the controller is idle and the Complete or Error Bit is set then an interrupt is generated immediately. The interrupt should be set only when resetting of the Idle Bit to Busy is done.

The Attention Interrupts are independent of the CCI, see Section 4.3.1.10.

4.3.8.4 LOCKOUT (LO) - CW7, BIT 4

The Lockout Bit, CW7 Bit 4, is used for in a Multiple CPU system configuration. When CW7 is read by a CPU the Lockout Bit will be set, by the controller. At power-up, or system reset, or at the end of a command sequence Lockout will be reset.

4.3.8.5 RE-TRY (RE-T) - CW7, BIT 5

Re-Try is set by the controller to indicate that the controller performed a Re-read of a sector during the last read command.

4.3.8.6 ECC CORRECTED (ECC) - CW7, BIT 6

ECC Corrected Bit is set by the controller to indicate that the controller corrected a data error in one or more sectors during the last Read Operation. The controller keeps a log of ECC corrections, for information on this log see Section 6.2.

4.3.8.7 CONTROLLER ERROR STATUS (CES) - CW7, BITS 7 - 15

These Bits are used to report any Error Status after a command has completed. Bits 8 through 15 are all set in the event of a Self-Test Error. Error information for each bit is defined as follows.

4.3.8.7.1 ABNORMAL COMPLETION (AC) - CW7, BIT 7

If the controller gets a Power On Reset, an I/O Reset, or a Power Failure warning then any disk operation is terminated and the Abnormal Completion Bit will be set.

4.3.8.7.2 MEMORY ERROR (ME) - CW7, BIT 8

The Memory Error Bit is set to indicate that system memory got an error when the controller was reading it. When (ME) comes up some operations will be terminated and any remaining data counts are not transferred.

4.3.8.7.3 DATA ERROR (DE) - CW7, BIT 9

During a Disk Read Operation if a Data Read Error is detected that cannot be corrected or Re-Read then Data Error will be set. The sector with the bad data will be transferred to system memory.

4.3.8.7.4 TILINE TIME-OUT (TT) - CW7, BIT 10

The TILINE Time-Out Bit is set to indicate that system memory did not answer the controller for a data transfer. When TT comes up some operations will be terminated and any remaining data counts are not transferred.

4.3.8.7.5 ID ERROR (IE) - CW7, BIT 11

The ID Error Bit is set if the controller cannot find the right Cylinder, Head and Sector Address from the Header Data coming from the disk. (IE) causes command termination.

4.3.8.7.6 RATE ERROR (RE) - CW7, BIT 12

This bit is not used by the controller and will only be set from a Self-Test Error, see Section 4.3.8.7.

4.3.8.7.7 COMMAND TIME-OUT (CT) - CW7, BIT 13

This Bit is set if an operation fails to complete in a pre-determined amount of time. This Bit is also set if a byte count greater then 510 is given for any Unformatted Command. CT causes command termination.

4.3.8.7.8 SEARCH ERROR (SE) - CW7, BIT 14

The Search Error Bit is set to indicate that the controller did not detect a Sync Character within an allotted amount of time while attempting to read from the disk. (SE) causes command termination.

4.3.8.7.9 UNIT ERROR (UE) - CW7, BIT 15

The Unit Error Bit is set when an operation is terminated because of a disk drive error. To see what drive error is active read CW0.

4.4 DETAILED COMMAND DESCRIPTIONS AND EXAMPLES

Of the fourteen Commands that the controller will perform most of them will use the standard definitions of the Control Words, as given in the Sections of 4.3.

For most of the Commands a Disk Address is required. This Address will be one of four types, Unit Select, Cylinder Address, Track Address, or a Sector Address with each type requiring the proceeding types, in the order given. They make up the following types:

TYPE 1 - UNIT SELECT - Is a Unit Select in CW6.

TYPE 2 - CYLINDER ADDRESS - Is of Type 1 plus a Cylinder Address in CW3.

TYPE 3 - TRACK ADDRESS - Is of Type 2 plus a Head Address in CW1.

TYPE 4 - SECTOR ADDRESS - Is of Type 3 plus a Sector Address in CW2.

If a Command requires system memory space then the Memory Address in CW5 and CW6 will point to the first byte of this space. The size of this Memory Space is defined by the Byte Count in CW4. The Address and Count must be an even byte address and count for the controller will transfer data in two byte words. All odd addresses and counts will be set down to the next even one.

The size of the Data Block to be moved, in a data transfer command, is determined by the even byte count in CW4. The controller will cross sector, head and cylinder address, in that order, until the transfer count is zero or an error ends the command.

See Table 4.1 for a list of the Commands and Command Codes with a detailed description and example given in the following Sections.

CW1, BIT 0	BIT 1	BITS 5	6	7	THE COMMAND
* X	X	0	0	0	STORE REGISTERS
* X	0	0	0	1	WRITE FORMAT
*** 1	1	0	0	1	ABSOLUTE WRITE FORMAT
*** 0	1	0	0	1	RELOCATE
* X	X	0	1	1	READ DATA
* X	X	0	1	1	WRITE DATA
0	X	1	0	0	UNFORMATTED READ
* X	X	1	0	1	UNFORMATTED WRITE
* X	X	1	1	0	SEEK
0	X	1	1	1	RESTORE
1	X	1	0	0	EXTENDED UNFORMATTED READ
** 1	X	1	1	1	T.I. SELFTEST
** 1	X	1	1	1	ECC ON/OFF
** 1	X	1	1	1	RE-TRY ON/OFF

NOTES:

* X= One or Zero

** These Three Commands have the same Command Code, see the Detailed Command Descriptions and Examples (Sections 4.4.10, 4.4.11, 4.4.12) for more information

*** Available only with the Alternate Track Mapping option.

LIST OF THE COMMANDS
AND COMMAND CODES

TABLE 4.1

4.4.1 STORE REGISTERS COMMAND

The Store Registers Command is used by the CPU to obtain up to three words of disk sizing parameters for the disk type configured at the selected unit address. One Store Registers Command needs to be done for each one of the four units that the controller will be controlling.

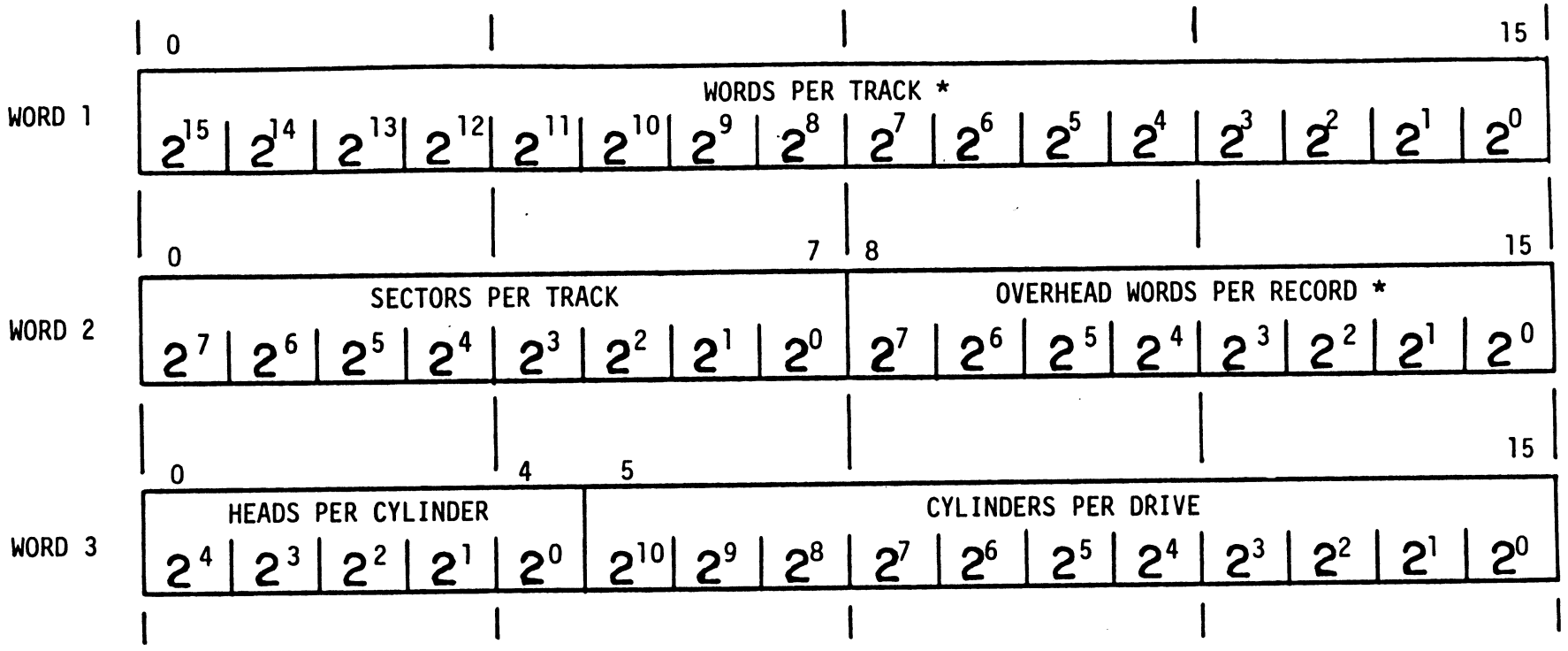
See Figure 4.2 for the format of the three words of a Store Registers Command. Word One contains the total number of Unformatted Words that can be recorded on a disk track. With a fixed format, as indicated by a value of zero in the words of overhead per logical record, Word One defaults to formatted words per track. Word Two, Bit 0 through 7, specify the number of sectors per track, and Bits 8 through 15 specify the number of overhead words per logical record. Word Three, Bits 0 through 4 specify the number of heads per cylinder, and Bits 5 through 15 specify the number of cylinders per drive.

A Store Registers Command will only transfer up to three words (six bytes), irregardless of a larger byte count in CW4, to the address specified in CW5 and CW6. Refer to Table 4.2 for an example of a Store Registers Command.

	SET-UP DATA IN HEX	COMMAND
CW0	0000	Clear Attention Mask Bits
CW1	0000	Store Registers Command; No Head Address is Required
CW2	0000	Not Used
CW3	0000	Not Used
CW4	0006	Transfer Byte Count = 6
CW5	1000	Starting TILINE Byte Address = 001000 Hex
CW6	0800	Select Unit 0
CW7	0000	Initiate Controller Operation; Completion Interrupt Disabled

EXAMPLE OF THE CONTROL WORDS
IN A STORE REGISTERS COMMAND

TABLE 4.2



NOTES

*THE 990 SMD + USES A FIXED SECTORS PER RECORD FORMAT SO THE WORDS PER TRACK = FORMATTED WORDS PER TRACK AND THE OVERHEAD WORDS PER SECTOR = ZERO.

FIGURE 4.2 FORMAT OF DATA FROM THE STORE REGISTERS COMMAND

4.4.2 WRITE FORMAT COMMAND

The Write Format Command is used to format a track on the selected Disk Unit. Only one complete track will be formatted per Write Format Command.

With the Alternate Track Mapping option at the start of the command, the controller will check if the selected track is relocated. If it is, the controller will seek to the alternate track.

Each sector of the track will be written with the framework that defines it as a uniquely addressable data record in the selected Disk Unit. The sector framework contains two fields, one for the Sector Address (the Header Field) and one for the Data (the Data Field), and the required gaps. See Sections 10.0 and 11.0 for more detailed format information. The Data Field will be filled with a fill word read from the specified memory address. Note that this Command will not change the Address or Count in CW4 through CW6.

Refer to Table 4.3 for an example of a Write Format Command.

	SET-UP DATA IN HEX	COMMAND
CW0	0000	Clear Attention Mask Bits
CW1	0102	Write Format Command; Head Address = 2
CW2	0100	One Sector per Record; Sector Address is not Required
CW3	01A2	Cylinder Address = 1A2 Hex
CW4	0000	Not Used
CW5	1200	The TILINE Byte Address for the Fill Word = 031200 Hex, See CW6 for Upper Part
CW6	0403	Select Unit 1; Upper Part of TILINE Address = 03
CW7	1000	Initiate Controller Operation; Completion Interrupt Enabled

EXAMPLE OF THE CONTROL WORDS
IN A WRITE FORMAT COMMAND

TABLE 4.3

4.4.3 ABSOLUTE WRITE FORMAT COMMAND

This command is available with Alternate Track Mapping option only.

The Absolute Write Format is used to format a track on the selected disk unit. Only one complete track will be formatted per command.

Relocated tracks are ignored and will be formatted as a normal track.

Each sector of the track will be written with the framework that defines it as a uniquely addressable data record in the selected disk unit. The sector framework contains two fields; one for the Sector Address (the Header Field), and one for the Data Field and the required gaps. See Sections 10.0 and 11.0 for more detailed format information. The data field will be filled with a fill word read from the specified memory address. Note that this command will not change the address or count in CW4 through CW6.

Refer to Table 4.4 for an example of an Absolute Write Format Command.

	SET-UP DATA IN HEX	COMMENTS
CW0	0000	Clear Attention Mask Bits
CW1	0103	Absolute Write Format Command; Head Address = 3
CW2	0100	One Sector per Record; Sector Address is not Required
CW3	0134	Cylinder Address = 134 Hex
CW4	0000	Not Used
CW5	4603	The TILINE Byte Address for the Fill Word = 024603 Hex, See CW6 for Upper Part
CW6	0802	Select Unit 0; Upper Part of TILINE Address = 02
CW7	1000	Initiate Controller Operation; Completion Interrup Enabled

EXAMPLE OF THE CONTROL WORDS IN AN ABSOLUTE WRITE FORMAT COMMAND

TABLE 4.4

4.4.4 RELOCATE COMMAND

This command is available with Alternate Track Mapping option only.

The Relocate Command is used to format a bad track with headers that point to an alternate track. The controller then seeks to the alternate track and formats that track to replace the bad one.

The alternate track address will be the first word pointed to by the memory address specified in CW5 and CW6. The second word will be the data word that the data field in both tracks will be filled with. Note that this command will change the byte count and TILINE address in the control words.

Refer to Table 4.5 for an example of a Relocate Command.

	SET UP DATA IN HEX	COMMENTS
CW0	0000	Clear Attention Mask Bits
CW1	4106	Relocate Command; Head Address = 6
CW2	0100	One Sector per Record; Sector Address is not Required
CW3	0321	Cylinder Address = 321 Hex
CW4	0002	Minimum Transfer Byte Count = 2
CW5	3500	The TILINE Byte Address for the Alternate Track Address and the Fill Word = 013500 Hex, See CW6 for Upper Part
CW6	0201	Select Unit 2; Upper Part of TILINE Address = 1
CW7	1000	Initiate Controller Operation; Completion Interrupt Enabled

EXAMPLE OF THE CONTROL WORDS
IN A RELOCATE COMMAND

TABLE 4.5

4.4.5 READ DATA COMMAND

The Read Data Command is used to get a block of data, up to 65536 bytes, from the selected disk unit. The controller will seek to the specified track address, find the starting sector then start transferring data to the Memory Space Addressed by CW5 and CW6. The size of the data block to be transferred is in CW4, the byte count. When the controller encounters the end of a Sector, Head or Cylinder and the transfer count is non-zero the controller will cross that boundary and continue transferring data.

With the Alternate Track Mapping option, if the controller encounters a track that has been relocated it will then read data from the alternate track.

Refer to Table 4.6 for an example of a Read Data Command.

	SET-UP DATA IN HEX	COMMENTS
CW0	0000	Clear Attention Mask Bits
CW1	0201	Data Read Command; Starting Head Address = 1
CW2	0104	One Sector per Record; Starting Sector Address = 4
CW3	0105	Starting Cylinder Address = 105 Hex
CW4	1500	Transfer Byte Count = 1500 Hex
CW5	8100	Starting TILINE Byte Address = 008100 Hex
CW6	0200	Select Unit 2; Upper Part of TILINE Address = 00
CW7	1000	Initiate Controller Operation; Completion Interrupt Enabled

EXAMPLE OF THE CONTROL WORDS
IN A READ DATA COMMAND

TABLE 4.6

4.4.6 WRITE DATA COMMAND

The Write Data Command is used to put a block of data, up to 65536 bytes, on to the selected disk unit. The controller will seek to the specified track address, find the starting sector then start transferring data from the Memory Space Addressed by CW5 and CW6 to the disk. The size of the data block to be transferred is in CW4, the byte count. When the controller encounters the end of a Sector, Head or Cylinder and the transfer count is non-zero the controller will cross that boundary and continue transferring data.

With the Alternate Track Mapping option, if the controller encounters a track that has been relocated, it will then write data to the alternate track.

If the data does not fill all of the last sector then that sector (the part without data) will be zero filled before going to the disk.

Refer to Table 4.7 for an example of a Write Data Command.

	SET-UP DATA IN HEX	COMMAND
CW0	0000	Clear Attention Mask Bits
CW1	0302	Write Data Command; Starting Head Address = 2
CW2	012B	One Sector per Record; Starting Sector Address = 2B Hex
CW3	02C3	Starting Cylinder Address = 2C3 Hex
CW4	2300	Transfer Byte Count = 2300 Hex
CW5	4206	Starting TILINE Byte Address = 054206 Hex, See CW6 for the Upper Part of the Address
CW6	0105	Select Unit 3; Upper Part of the Starting TILINE Byte Address = 05
CW7	1000	Initiate Controller Operation; Completion Interrupt Enabled

EXAMPLE OF THE CONTROL WORDS
IN A WRITE DATA COMMAND

TABLE 4.7

4.4.7 UNFORMATTED READ COMMAND

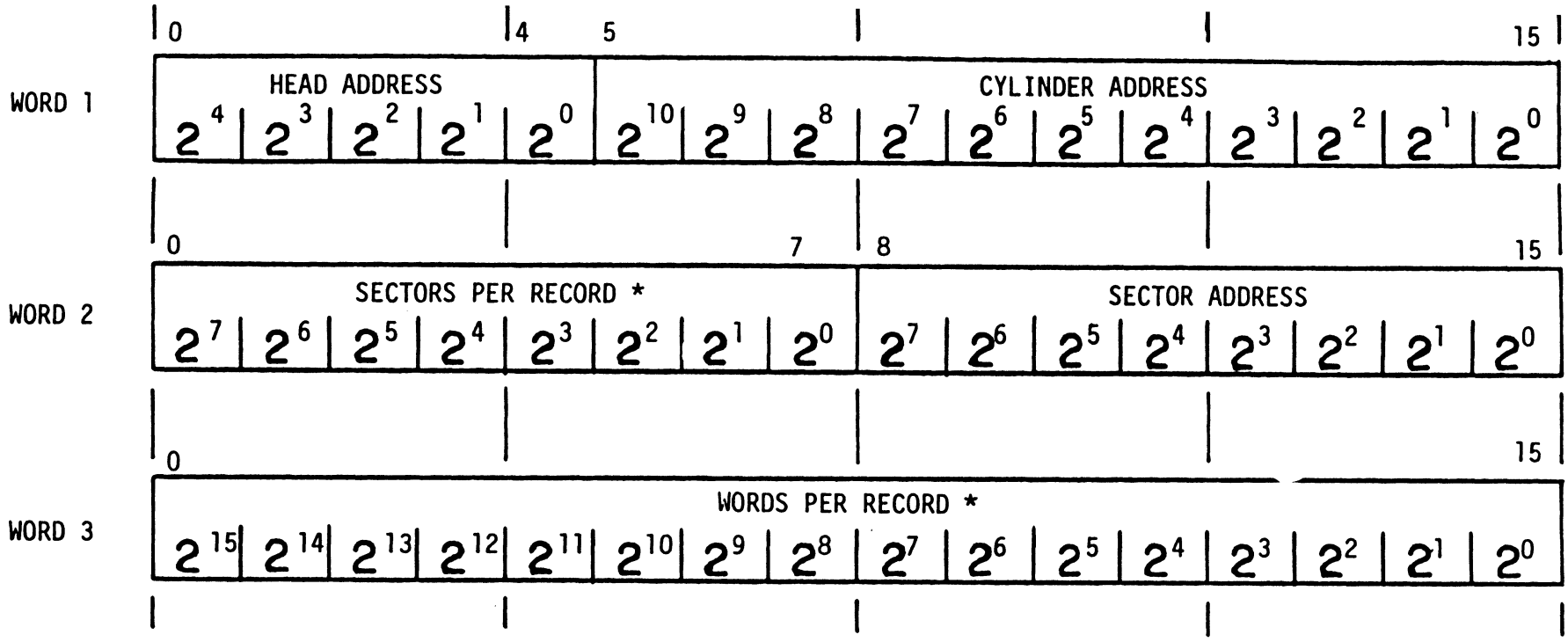
The Unformatted Read Command is used to get sector format information per track. This Command will return up to three words. The first word contains the Head and Cylinder Addresses. The second word contains the Sectors per Logical Record Number (for a fixed format this number is 01 Hex) and the Sector Address. The third word contains the Record Word Count. If desired a genuine unformatted Read from the disk may be done, for this use the Extended Unformatted Read Command.

Refer to Figure 4.3 for the data format of the three words returned by this Command and Table 4.8 for an example of an Unformatted Read Command.

	SET-UP DATA IN HEX	COMMAND
CW0	0000	Clear Attention Mask Bits
CW1	0401	Unformatted Read Command; Head Address = 1
CW2	0100	One Sector per Record; the Physical Sector Address = 0
CW3	0102	Cylinder Address = 102 Hex
CW4	0006	Transfer Byte Count = 6
CW5	2000	Starting TILINE Byte Address = 002000 Hex
CW6	0400	Select Unit 1
CW7	1000	Initiate Controller Operation; Completion Interrupt Enabled

EXAMPLE OF THE CONTROL WORDS IN AN UNFORMATTED READ COMMAND

TABLE 4.8



NOTE

*THE 990 SMD+ USES A FIXED SECTOR FORMAT SO THE SECTORS PER RECORD = WORDS PER SECTOR AND THE SECTORS PER RECORD = ONE.

FIGURE 4.3 FORMAT OF DATA FROM THE UNFORMATED READ COMMAND

4.4.8 EXTENDED UNFORMATTED READ COMMAND

The Extended Unformatted Read Command is used to read data (up to 510 bytes) from the selected disk, irregardless of the sector format or sector boundaries. The controller will seek to the specified track address, find the starting sector then start transferring data from the disk. Note that the controller needs to find a sync byte before data can be transferred to the system, and the data to be transferred starts just after the sync byte. This command will not cross track boundaries.

Refer to Table 4.9 for an example of an Extended Unformatted Read Command.

	SET-UP DATA IN HEX	COMMAND
CW0	0000	Clear Attention Mask Bits
CW1	8402	Extended Unformatted Read Command; Head Address = 2
CW2	0100	One Sector per Record; the Physical Sector Address = 0
CW3	0123	Cylinder Address = 123 Hex
CW4	0300	Transfer Byte Count = 300 Hex
CW5	2200	Starting TILINE Byte Address = 002200 Hex
CW6	0800	Select Unit 0
CW7	1000	Initiate Controller Operation; Completion Interrupt Enabled

EXAMPLE OF THE CONTROL WORDS IN AN EXTENDED UNFORMATTED READ COMMAND

TABLE 4.9

4.4.9 UNFORMATTED WRITE COMMAND

The Unformatted Write Command is used to write data (up to 510 bytes) to the selected disk, irregardless of the sector format or sector boundaries. The controller will seek to the specified track address, find the starting sector then write a Lead Gap, a Synchronization Character, and the Block of Data, an ECC Field, and zeros to the next sector mark. This Command will not cross track boundaries.

Refer to Table 4.10 for an example of an Unformatted Write Command.

	SET-UP DATA IN HEX	COMMAND
CW0	0000	Clear Attention Mask Bits
CW1	0500	Unformatted Write Command; Head Address = 0
CW2	0100	One Sector per Record; the Physical Sector Address = 0
CW3	00C2	Cylinder Address = 0C2 Hex
CW4	0250	Transfer Byte Count = 250 Hex
CW5	1000	Starting TILINE Byte Address = 001000 Hex
CW6	0100	Select Unit 3
CW7	1000	Initiate Controller Operation; Completion Interrupt Enabled

EXAMPLE OF THE CONTROL WORDS
IN AN UNFORMATTED WRITE COMMAND

TABLE 4.10

4.4.10 SEEK COMMAND

The Seek Command is used to start the heads, of the selected disk unit, moving to the Cylinder Address specified in CW3. Once the controller has started the heads moving it will go back to the Idle Mode (note that the Head move may not be done at this time) however, the controller may be given another command. To find out if the Heads are done moving use the Attention Bits or Attention Interrupt Mask in CW0.

Seeks are not performed on a drive that has more than one Logical Unit in it (multiple volume drives).

Refer to Table 4.11 for an example of a Seek Command.

	SET-UP DATA IN HEX	COMMAND
CW0	0004	Set Attention Mask Bit for Unit 1 (Attention Interrupt Enabled)
CW1	0600	Seek Command
CW2	0000	Not Used
CW3	0124	Cylinder Address = 124 Hex
CW4	0000	Not Used
CW5	0000	Not Used
CW6	0400	Select Unit 1
CW7	1000	Initiate Controller Operation; Completion Interrupt Enabled

EXAMPLE OF THE CONTROL WORDS IN A SEEK COMMAND

TABLE 4.11

4.4.11 RESTORE COMMAND

The Restore Command is used to re-initialize a disk drive that has an Unsafe or Seek Incomplete Error Status, in CW0. This Command may be sent to any Unit at any time to try to clear a Unit Error. Once the controller has started the re-initialization it will go back to the Idle Mode but the drive is doing a Long Seek to cylinder zero. When the controller is back into the Idle Mode it may be given another Command. To find out if the Long Restore Seek to zero is done use the Attention Bits or Attention Interrupt Mask in CW0.

A Restore on a drive which is two logical units will result in both logical units being re-initialized.

	SET-UP DATA IN HEX	COMMAND
CW0	0008	Set Attention Mask Bit for Unit 0 (Attention Interrupt Enabled)
CW1	0700	Restore Command
CW2	0000	Not Used
CW3	0000	Not Used
CW4	0000	Not Used
CW5	0000	Not Used
CW6	0800	Select Unit 0
CW7	1000	Initiate Controller Operation Completion Interrupt Enable

EXAMPLE OF THE CONTROL WORDS IN A RESTORE COMMAND

TABLE 4.12

4.4.12 T.I. SELF-TEST COMMAND

The T.I. Self-Test Command is a NOP Command to the 990 SMD+ Controller. No operation is performed but the returning of a Go/No-Go Status. For more information about CSI 990 SMD+ Self-Test see Section 5.0.

Refer to Table 4.13 for an example of a T.I. Self-Test Command.

4.4.13 ECC ON/OFF COMMAND*

The ECC On/Off Command is used to Enable or Disable the ECC Correction Function of the controller. Refer to Section 6.0 for more information on the ECC Correction Function of the Controller.

The ECC On/Off is a sub-function of the T.I. Self-Test Command. Refer to Table 4.13 for an example of an ECC On/Off Command.

4.4.14 RE-TRY ON/OFF COMMAND*

The Re-Try On/Off Command is used to Enable or Disable the Re-reading Function of the Controller. The number of Re-reads the controller will try per sector is two.

The Re-Try On/Off is a sub-function of the T.I. Self-Test Command. Refer to Table 4.13 for an example of a Re-Try On/Off Command.

*NOTE A power on Reset or IORESET will Enable the ECC and Re-Try functions.

	SET-UP DATA IN HEX	COMMAND
CW0	0000	Clear Attention Mask Bits
CW1	8700	T.I. Selftest*
CW2	0000	Not Used
CW3	*	The Test Select Bits
CW4	0000	Not Used
CW5	0000	Not Used
CW6	0000	Not Used
CW7	0000	Initiate Controller Operation; Completion Interrupt Disable

NOTE:

*For ECC and Re-Try Commands

CW3 = 0E0F - ECC ON

CW3 = 0E00 - ECC OFF

CW3 = 0F0F - RE-TRY ON

CW3 = 0F00 - RE-TRY OFF

EXAMPLE OF THE CONTROL WORDS IN A T.I. SELF-TEST; ECC AND RE-TRY ON/OFF COMMANDS

TABLE 4.13

5.0 990 SMD+ SELF-TEST

The controller features extensive self-testing which is run upon power-up or whenever the controller receives a Reset, either from the Reset switch on the programmer panel or from a Reset (RSET) instruction.

When the self-test begins, the controller is placed in the Busy Mode and the Controller Busy and Fault LEDS become lit. If all tests pass successfully with no errors, all LEDS will go out, and the controller will enter the Idle Mode.

5.1 SELF-TEST ERRORS

If any errors occur during the Self-test, the fault LED will remain lit and the Error code LED will blink, displaying a code to indicate the section of the test in which the failure occurred. See Section 5.1.2 for an explanation of the Error Display Codes.

While displaying the Error Code, the controller is placed in an Idle Mode for slave reading and writing of the control words. The Error Code multiplied by 2 is returned in Control Word 2 and the lower byte of Control Word 7 is set to OFF Hex.

5.1.1 ERROR DIAGNOSIS

The five LEDS on the front of the controller board from left to right represent Interrupt Pending (yellow), Controller Busy (green), Command Time-Out, Controller Fault and Error Code. Section 9.2 contains a complete description of these indicators.

If a Section of the Self-test fails, Fault and Error Code LEDS should be lit. Refer to the follwing Section for Error Code explanations. If the controller is unable to display an Error Code, the other LEDS may be examined to help determine the nature of the malfunction.

If no LEDS are lit and the controller's control words cannot be accessed, remove power from the chassis and check to see that the controller board is seated firmly in the chassis slot. Verify that power is being supplied to the slot the controller occupies, either by inserting another board or measuring that +5 0.25 vdc is present on the controller.

If Command Time-Out is the only LED lit, the controller's microprocessor is unable to execute basic instruction stepping, test conditions and may be in a Halt state or looping near the start of the microprogram.

If Busy and Fault become lit, and Command Time-Out approximately 1/2 second later, the self-test may be suspended in a loop or the controller's microprocessor held in a Wait state.

5.1.2 ERROR DISPLAY CODES

When a section of the self-test cannot pass successfully, the controller will display an Error Code by blinking the Error Code (right-most) LED to indicate the section of the test which failed. This code may be used to help in isolating the area of the malfunction to a particular region of the controller.

ERROR CODE	FAILURE DESCRIPTION
2 Blinks	MICROPROCESSOR REGISTER TEST FAILURE: Unable to perform arithmetic functions, move data between registers.
3 Blinks	DATA BUS, LITERAL DATA WORD, ARITHMETIC TEST CONDITION FAILURE: Could not transfer and successfully test for correct data read from the firmware bus to the microprocessor over the controller data bus.
4 Blinks	MICROPROGRAM ADDRESS SEQUENCER TEST FAILURE: Unable to sucessfully execute various address control instructions, load and use internal counter.
5 Blinks	CONTROLLER RAM TEST FAILURE: Unable to properly address, increment address, write and read correct data from the controller's random-access memory over the controller's data bus.
6 Blinks	DISK FORMAT CONTROL SEQUENCER TEST FAILURE: Unable to simulate a disk write command without errors or calculate and read correct ECC results.

6.0 ECC CORRECTION AND RE-TRY

To insure high data integrity, the 990 SMD+ performs on-board error checking and correcting on each sector of data as it is read from the disk. An error correcting code (ECC) with a 32-bit character is used, capable of correcting burst errors up to 11 bits in length.

Three polynomials are used:

Header CRC - 16 Bit

$$X^{16} + X^{15} + X^{2} + 1$$

Write Data (Generator)

$$X^{32} + X^{23} + X^{21} + X^{11} + X^{2} + 1$$

Read Data (Factored version of Generator)

$$(X^{11} + X^{2} + 1)\ (X^{21} + 1)$$

When the controller detects that an error in data integrity has occurred, it will attempt to correct the bad section of data and restore it to memory. If the correction is successful, the ECC corrected bit (bit 6 of Control Word 7) is set and the Read command is resumed. The controller also records pertinant information of the correction in a log in controller RAM (Section 6.2).

If the error is found to be uncorrectable, the controller will re-read the sector a certain number of times in an attempt to obtain correctable data. If all attempted re-tries fail, the Data Error bit (bit 9 of Control Word 7) is set, and the Read command is terminated.

6.1 ECC AND RE-TRIES ON/OFF

The CPU may disable or enable the controller's ability to correct data and/or re-read sectors in which ECC errors are detected. This is done with an Extended Restore command. See Sections 4.4.11 and 4.4.12 for full descriptions of these commands. Both functions are enabled upon controller initialization.

When detecting an ECC error, the controller first checks to see if the ECC corection function is enabled. If disabled, it will then check to see if re-tries are enabled. If both functions are disabled, the controller will set the Data Error bit and terminate the Read command.

6.2 ERROR CORRECTION LOG

Each time an ECC correction on read data is performed by the controller, it records the cylinder, head and sector addresses of the disk, the bit offset of the error from the beginning of the sector, and an 11 bit error burst mask which, when exclusive-or'd with the error burst, results in corrected data.

The log is used by the 990 SMD+ Reliability and Surface Analysis programs to inform the user of the location and extent of any media defects that may exist on the disk surfaces.

7.0 DIAGNOSTIC AND RELIABILITY

The Diagnostic Support for the 990 SMD+ consists of a Reliability Program. Attached to it is a copy of the ZETACO Debugger Utility. The purpose of the program is to test for proper operation and reliability of the 990 SMD+ Controller. If this is to be done it must be assumed that the drive is not at fault, although many of the errors and their displays may help in determining a disk drive malfunction. The program will look for a 911 at CRU address >100 first and if one does not exist, it will expect a 931 CI 403 at >F980 on unit 0.

7.1 ZETACO DEBUGGER UTILITY

The ZETACO Debugger (Debug for short) is a program debugging utility that can be a very helpful subsystem. It consists of Memory Modification and Display Commands as well as Program Control Commands.

7.1.1 DEBUG COMMAND DESCRIPTIONS

7.1.1.1 MM - EXAMINE AND/OR MODIFY MEMORY

Allows the User to examine and/or modify any Memory location (0-64K).

7.1.1.2 MW - EXAMINE AND/OR MODIFY WORKSPACE REGISTERS

Allows the User to examine and/or modify the Workspace Registers in use at the time a breakpoint is hit.

7.1.1.3 SB - SET AND/OR DELETE BREAKPOINT

Allows the User to set a Breakpoint at any one word location. Upon entry of Command, the previous breakpoint is cleared.

7.1.1.4 DM - DISPLAY A BLOCK OF MEMORY

Allows User to specify a Block of Memory to be displayed one page at a time.

7.1.1.5 SE - START EXECUTION

Allows User to start Program Execution at a specified location using a specified workspace.

7.1.1.6 CB - CONTINUE FROM BREAKPOINT

Allows the User to continue execution from a Breakpoint and/or set a new Breakpoint. NOTE: Upon entry of the Command the old Breakpoint is cleared. The new Breakpoint cannot be the same as the old one.

7.1.1.7 FM - FILL MEMORY

Allows the User to fill a specified area of memory.

7.1.1.8 TL - TEST LOOP

Allows User to continuously Read or Write any Memory location.

7.1.1.9 SO - SET OFFSET

Allows the user to set an Offset to be added to all Memory Reference Commands.

7.1.1.10 RE - RETURN TO TEST

Allows User to return to the exact location Debug was called from in a program.

7.1.1.11 CC - CRU COMMANDS

Allows User to execute any CRU Command.

7.1.1.12 LC - LIST COMMANDS

Allows User to get a list of all available Commands.

7.1.1.13 ET - EXECUTE TEST

Allows User to start execution of the attached program.

7.1.1.14 MR - MODIFY TPCS REGISTERS

Allows User to modify TPCS Registers. This Command loops on the eight locations starting at the specified address.

7.1.2 DEBUG USAGE SUGGESTIONS AND NOTES

The interrupts are disabled down to Level 1 during the execution of the debugger.

The MR Command is very useful for giving instructions to a TILINE Device and then checking the results.

/ - This entry will cause some Commands to not modify the present location but display the next.

SP - This entry will exit all Commands except DM where it will get the next page.

'RETURN' - This entry will exit all Commands if nothing proceeds it. It is used to terminate all entries.

← - This entry will Backspace one location and allow re-entry of the last entered character.

BUFF - This will automatically use the Buffer Address supplied by the attached program as an entry. It will work on DM, MM, MR and FM.

7.2 990 SMD+ RELIABILITY

The purpose of the 990 SMD+ Reliability (Reli for short) is to operate the entire subsystem in a manner which is close to that in which the system itself would operate it in but still retain the ability to display and log error conditions in a way in which they can be useful.

7.2.1 RELIABILITY COMMAND DESCRIPTIONS

7.2.1.1 SHOW PORT SETTINGS

This is a very special Command. This Command will allow you to read extensive technical information from the controller. On the first page will be the revision level and subset information and a list of Drive types available in the EPROM. At the bottom is a list of how each port is set for Drive type. This will allow you to verify that the switches are properly set. By entering a unit selection you will be able to see specific information about the unit you selected and its selected Drive type.

7.2.1.2 FORMAT DISK

The Disk will be formatted using the Store Registers information. This is simply a quicky format to enable running of the reliability. If an error occurs it will be re-tried and displayed.

7.2.1.3 SURFACE ANALYSIS

This routine is used to find and log bad tracks for running an error-free pass of the reliability. The entire disk is written, then read and the data checked. If an error occurs the operation is re-tried. If after all the re-trys, and on a read, the error persists it is logged as a bad track. The bad track map is then put on Track 0, Sector 1 with each word containing a Track Number. A 1234 Hex is then written into Track 0, Sector 0 in Word 0A4 Hex to signify that a bad track map has been built. NOTE: This map is not of the TI form so as to prevent the User from using it as a substitute for the TI Format and Initialization.

7.2.1.4 COMMAND STRING UTILITY

The Command String Utility is a routine that will allow you to build up a string of 1 - 20 Commands to be executed in order. A loop capability is also available as well as error displaying during running.

7.2.1.5 SEEK EXERCISER

This routine will simply do seeks to a drive and report the errors. It obviously will not do any real operation on any multi-volume drives. The converging pattern seeks from 0 to the max, then to 0 + 1 to max -1 etc.

7.2.1.6 ECC ON/OFF

This call will turn Off/On the ECC Correction Logic in the controller. Remember, Reset always turns it on.

7.2.1.7 SOFTWARE RE-TRYS ON/OFF

This call will allow you to set any count of Software Re-trys between 0 - 8. It is reset to 8 at program restart.

7.2.1.8 TRACE ON/OFF

This call will allow you to set a trace count from zero to six and then enable or disable the trace option. Trace is an option which will display the starting and ending TPCS Registers when an error occurs. If the trace count is set for two or more the history of operations can be determined.

7.2.1.9 RELIABILITY

This routine is the heart of this program. Its purpose is to randomly select a Drive, do a Seek-Write-Read combination, and then check the data. All errors are displayed and most are logged as hard (errored on all re-tries) or soft (recovered on a re-try). Random Seeks and Restores are dispersed among the other commands at random. If a unit gets an unrecoverable error it is taken off the list of available units and the other units continue to run. If all available units are removed the program will stop execution of the reliability.

On detection of a controller data error the data received is tested up to the actual amount transferred in order to show the erroring data.

On detection of an ECC Correction the program will interrogate the controller to show the corrected data error.

Refer to the Flow Charts for further information.

7.2.2 RELIABILITY SPECIAL FEATURES

7.2.2.1 SPECIAL KEYS

During execution of the various routines the numeric keys can be used for control. The "9" key will always be hit to display a list of the keys that can be used at that time. The "0" key will always jump immediately to the debugger. Other keys are:

1 - Restart Program

2 - Get New Command String

3 - Exit to Debug

4 - List Error Totals

5 - Enable/Disable Trace

7.2.2.2 DISPLAY STOP

During a display to the screen the display can be halted by hitting a space key. Hitting any other key will restart the display.

7.2.3 RELIABILITY ERROR REPORTING

7.2.3.1 UNIT NUMBER

This is the Unit under test at the time of error.

7.2.3.2 CYLINDER/HEAD/SECTOR

These are the ending values after operation completion except on Error 1. In that case they are the Starting Values.

7.2.3.3 ERROR

This value will tell you what the error is. The errors are prioritized so that a lower value error proceeds a larger value error. Refer to Table 7.1.

15 - Time Out waiting for ATTN

14 - Time Out waiting for INTR

13 -

12 - ECC Corrected

11 - Controller Executed Re-Read

10 - Search Error

0F - Command Timer

0E - Rate Error

0D - ID Error

0C - TILINE Time Out

0B - Controller Data Error

0A - Memory Error

09 - Abnormal Completion

08 -

07 - Seek Incomplete

06 - Unsafe

05 - Write Protect

04 - Not Ready

03 - Offline

02 - Improper Error Status

01 -

00 - No Error

RELIABILITY ERROR LIST

TABLE 7.1

7.2.3.4 COMMAND

This is a code that relates to the Command in execution. It is a copy of TPCS 1.

7.2.3.5 ADDRESS

This is the Address in the controller at the operation completion.

7.2.3.6 STATUS

This is the value of TPCS 7 on operation completion.

7.2.3.7 TPCS REGISTERS

These are the starting and ending values of the controller registers.

7.2.3.8 RE-TRYS - HARD

Re-trys will specify the number of software re-trys before the operation was successfully completed. Hard means that the operation failed on all software re-trys.

7.2.3.9 DATA COMPARE ERROR

If the buffer compare routine finds an error and it is not testing on a controller data error or an ECC Display it will display the erroring data and a trace (if enabled). If it is doing a data error check or an ECC Display it will only display the erroring data.

Data format consists of the address in the good data buffer, the good data, the bad data, the word count from the buffer start and a total error count. Only the first three errors are displayed.

7.3 LOADING RELIABILITY

7.3.1 BOOTING

Follow the TI Tape Booting Procedure to load the Reliability program. The program is a sequential object file designed to be loaded at address 0A0 Hex.

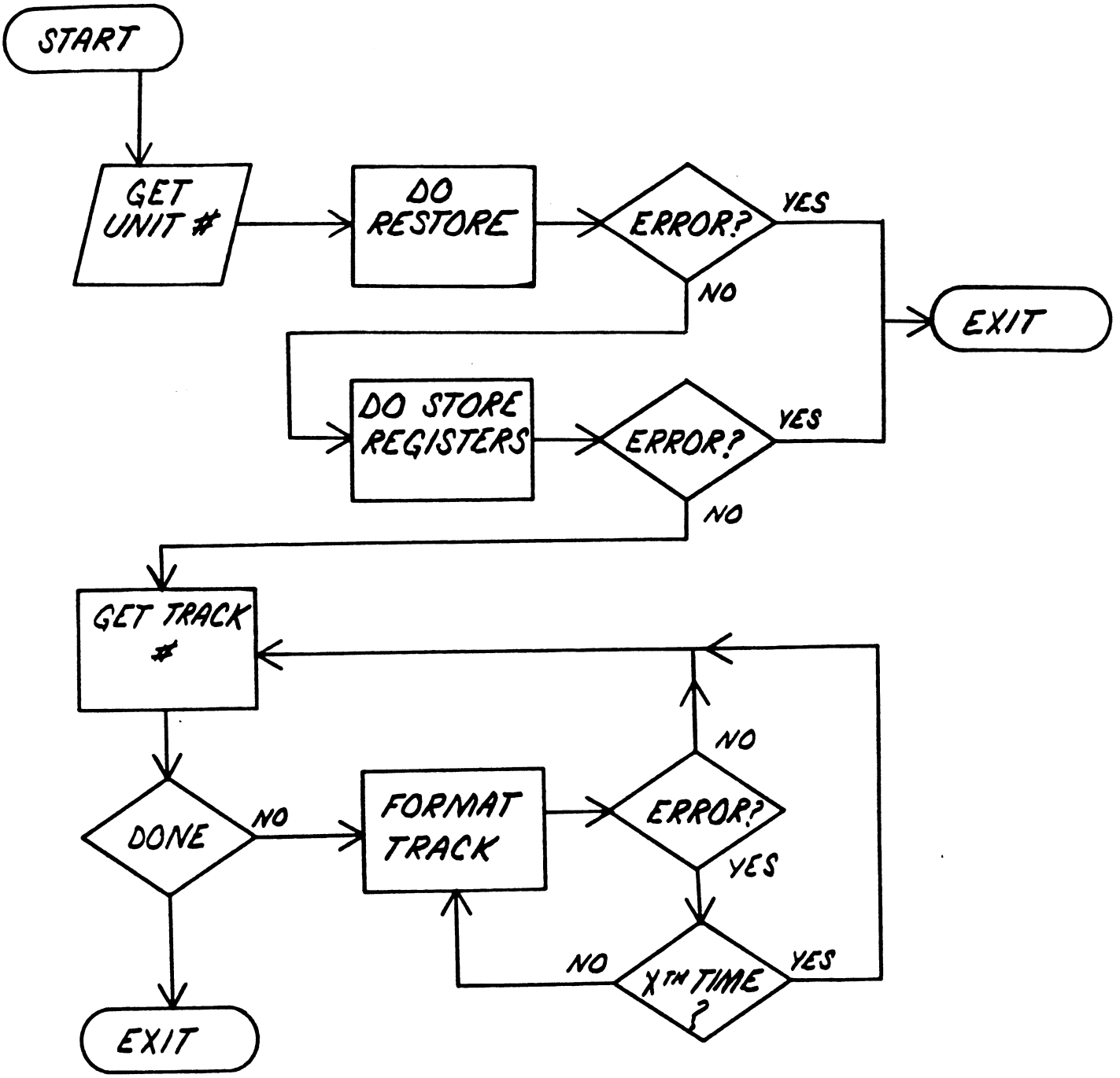
7.3.2 RUNNING

The program will come up running automatically.
The program will print "ZETACO 990 DISK RELIABILITY-REVXX".
To proceed hit carriage return.

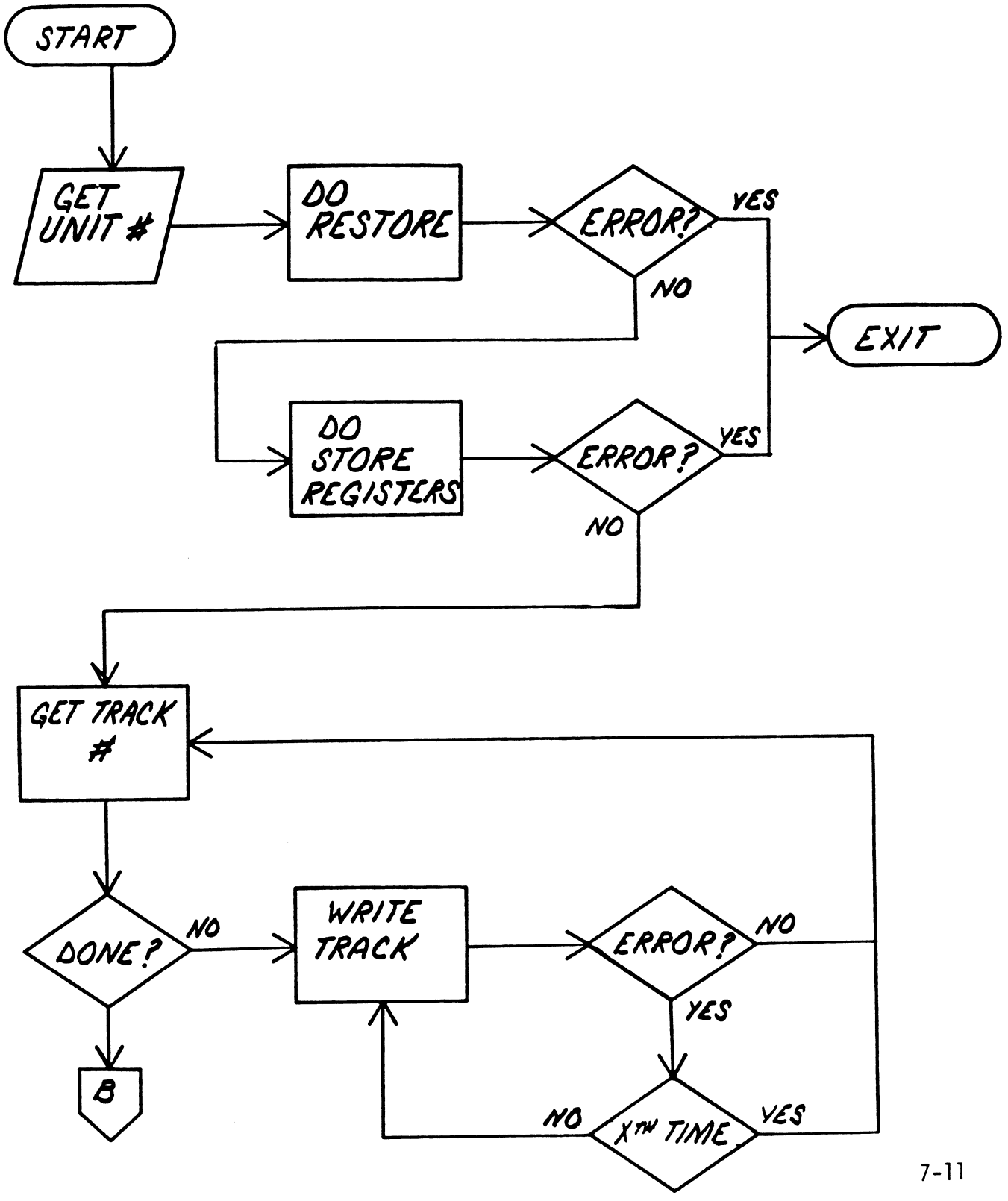
7.4 FLOW CHARTS

The basic Flow Charts for the Main Routines in the Reliability is as follows.

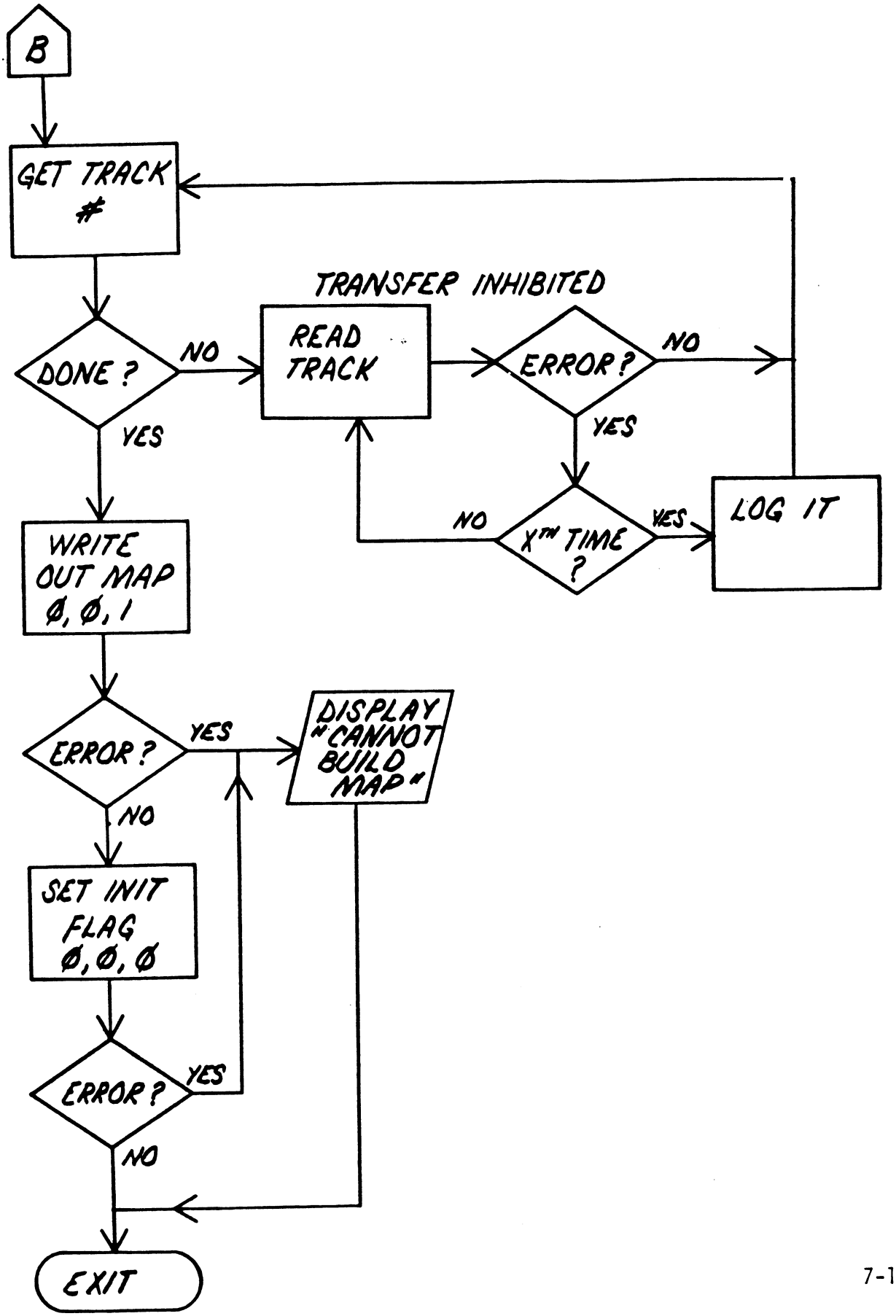
FLOW CHART FOR FORMAT DISK



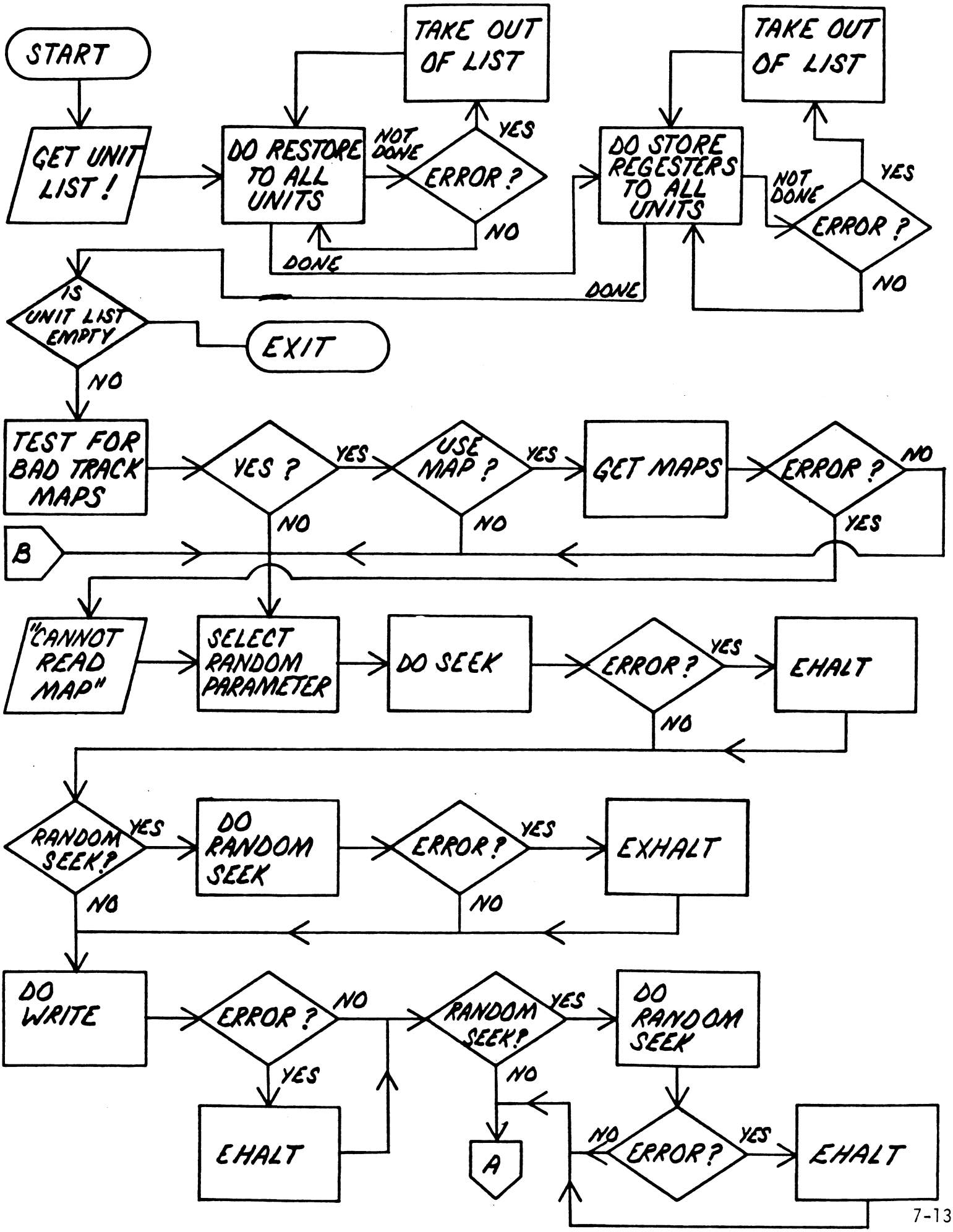
FLOW CHART FOR INITIALIZE DISK PART 1 of 2



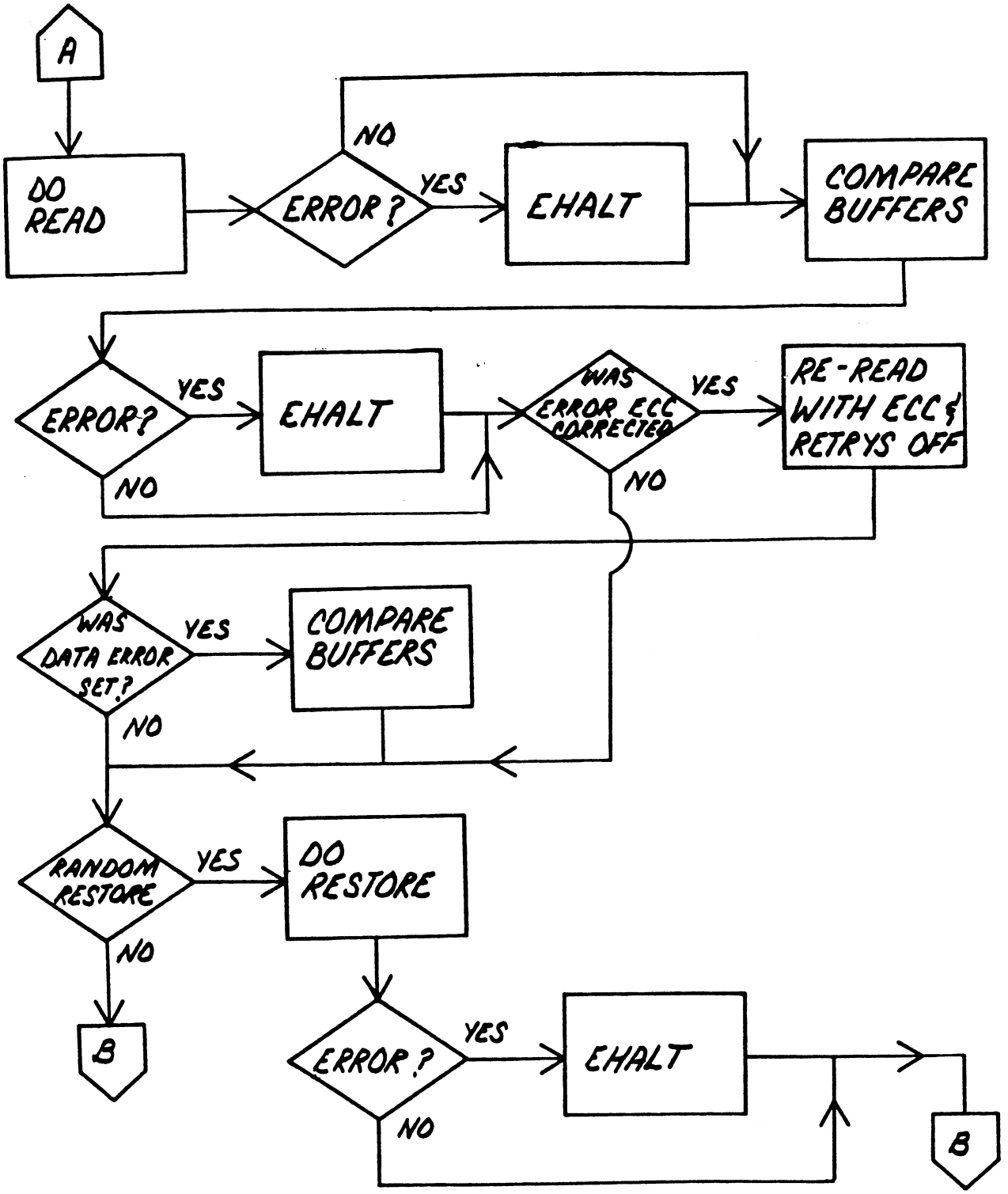
FLOW CHART FOR INITIALIZE DISK PART 2 of 2



FLOW CHART FOR RELIABILITY PART 1 of 3

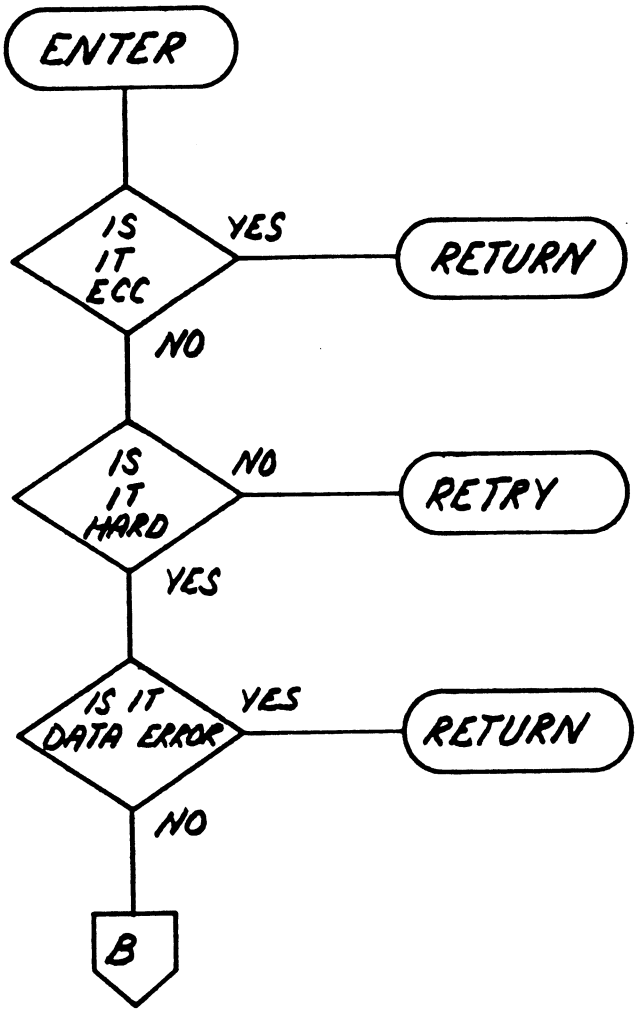


FLOW CHART FOR RELIABILITY PART 2 of 3



FLOW CHART FOR RELIABILITY PART 3 of 3

EHALT



8.0 CONFIGURATION WORKSHEET

The 990 SMD+ will work with most Disk Drives that use the Control Data Corporation (CDC) Storage Module Drive (SMD) interface. Of the large number of disk drives with this interface only 15 different types of drives may be configured at a time. However, more than 15 different Models of disk drives may be supported at a time.

EXAMPLE: The Drive Type Code of 2.00 may be used with the following Disk Drives:

CDC 9762
CDC 9730-80
CDC 9710
Century T-82
Kennedy 5380
Kennedy 7380
Tecstor 85

These seven Drives belong to just one Drive Type.

The 990 SMD+ is equipped with two configuration EPROMS that contain the information necessary for the 15 different drive types (and is called a subset). To change subsets one would just change the EPROMS to the subset of disk drives desired. For more information on changing subsets call the ZETACO Sales Department.

Addendum 1 contains the information about the subset that the controller is equipped with. This information is as follows:

- -The SUBSET CODE and REVISION LEVEL
- -The DISK DRIVES SUPPORTED
- -(SW4, SW3, SW2, SW1) The configuration switch settings
- -(BANK) The EPROM BANK NUMBER
- -(SECT) The Sectors per Track
- -(SIZE MB) The Formatted Size in M-Bytes
- -(DT CODE) The Drive Type Code, for ZETACO use
- -(MAP CYL) Mapped Cylinders Available for Alternate Track Mapping option only.

8.1 FILLING OUT THE CONFIGURATION WORKSHEET

The Worksheet is Table 8.1.

FIRST: Write in the disk drives to be used at each unit, part 1A or 1B.

-NOTE that the system disk should be put at Unit 0.

-PART 1A: is for use with single volume disk drives, that is drives with only one disk in a physical unit. Either one removable disk or one fixed disk but not both.

-PART 1B: is for use with multiple volume disk drives that is drives with two disks in a physical unit. This type of disk drive will use two consecutive unit addresses on the controller. In Addendum 1 under DISK DRIVES SUPPORTED for multiple volume drives it will say if it is a (Removable or Fixed), (Upper Unit or Lower Unit) volume. A multiple volume drive can use only the following configuration:

UNIT 0	UNIT 1	UNIT 2	UNIT 3
<Lower Unit:Upper Unit>			
	<Lower Unit:Upper Unit>		
		<Lower Unit:Upper Unit>	
<Lower Unit:Upper Unit>		<Lower Unit:Upper Unit>	

-NOTE that if no drive is to be put at a unit address then write NONE into part 1A for that unit.

SECOND: For each unit write in the BANK NUMBER, CONFIGURATION SWITCH SETTINGS and the SECTORS/TRACK. The information will be found in Addendum 1.

-JUST look under DISK DRIVES SUPPORTED for the drive and the other information will be on either side of it.

-NOTE that the right drive type (BANK) is selected for multiple volume drives (lower Unit) or (Upper Unit).

8.2 THE RECORD SELECT SWITCH

If the controller is equipped with two records, (see Addendum 1)*, then all drive types selected must come from just one record at a time. The record select switch is used to select one of the records, (refer to Figures 1.1 and 3.4).

THE SWITCH	THE RECORD SELECTED*
ON ***	The Lower Record
OFF ---	The Upper Record

*NOTE: If it is a single record set, then the Addendum will have Banks 1 through 15. If it is a multiple set, it will have Banks 1 through 30.

**NOTE: See Figure 3.4

TILINE ADDRESS: _____ INTERRUPT LEVEL: _____ CHASSIS SLOT: _____

	UNIT 0	UNIT 1	UNIT 2	UNIT 3
1A: Single Volume Disk Drives				
1B: Multiple Volume Disk Drives	☐ Lower Unit	Upper Unit ☐ Lower Unit	☐ Lower Unit Upper Unit	Upper Unit
2: The Bank Number				
3: Configuration Switch Settings	SW4 SW3 SW2 SW1	SW4 SW3 SW2 SW1	SW4 SW3 SW2 SW1	SW4 SW3 SW2 SW1
4: Sectors/Track				
5: For Use With Multiple Configuration Records Only, Refer to Addendum 1	THE RECORD SELECTED ☐ Lower Record - Record Select Switch = ON ☐ Upper Record - Record Select Switch = OFF The Lower Record Code _____ The Upper Record Code _____			

CONFIGURATION WORKSHEET

Table 8.1

9.0 SWITCHES, JUMPERS AND INDICATORS OF THE 990 SMD+ CONTROLLER

To locate the switches, jumpers and indicators refer to Figure 1.1.

9.1 SWITCHES OF THE 990 SMD+

Of the five switches four of them are four-bay DIP switches used to configure the controller. These switches are called Configuration Switches, with one switch per each one of the four "B" cable headers. The configuration switches will select one of the 16 banks in the configuration EPROMS.

Refer to Section 3.3.3, Figure 3.5 and Table 3.2 for more information on these four switches.

The fifth switch is the Address Switch and is an eight-bay DIP switch. The first six switch bays are used to select the controllers base TILINE Address (DX10's primary disk address is 0F800 Hex). Address switch bay seven is used when the configuration EPROMS are 2732's as the upper most address bit (refer to Sections 3.3.3.1 and 8.2). Switch bay eight is used to enable/disable the hardware time out timer, (ZETACO use only).

For more information on the TILINE address switch see Section 3.3.1, Figure 3.4 and Table 3.1.

9.2 INDICATORS OF THE 990 SMD+

The 990 SMD+ controller has five LED indicators, three red, one green and one yellow.

The yellow LED is on when the controller has an active interrupt going to the system. If the yellow LED is on all the time then the system is not answering the controller's interrupt.

The green LED is on only when the controller is busy executing a command or running self-test. The LED is known as the busy LED.

The three red LEDS are used for error indicators. The center LED is the controller fault LED and will be on when running self-test. When self-test passes successfully (no errors) this light will go out. If there is a fault then this LED will stay on and an error code will be displayed. The error code LED is the red LED farthest from the green busy LED, see Section 5.1.2 for more information on the error code LED. The red LED next to the green busy LED is the command time-out LED. The command time-out LED is on if the controller is not running or if not able to run self-test.

9.3 JUMPERS OF THE 990 SMD+

Of the nine jumpers on the controller only four are to be changed in the field. The other five are for use by ZETACO only, used in PC Board configuration and check-out.

W11-1 & 2	To be used to change the interrupt from the P2-connector over to the P1-connector, refer to Section 3.3.2.
W14-1	IS FOR ZETACO USE ONLY. To be used to override address switch number eight, for checkout only. This jumper should be closed for use.
W17-1 & 2	IS FOR ZETACO USE ONLY. To enable the use of 2732 in place of 2716 for the configuration EPROMS. Refer to Section 3.3.3.1.
W23-1 & 2	IS FOR ZETACO USE ONLY. To be used to change the disk base unit address. This is a ZETACO configurable option.
W23-3 & 4	Some disk drives use over 1024 cylinders and need a Tag-Bit-10 however, some drives will ground this line in the cable. The jumpers are for the drives that ground the lines and must be opened for them.

9.3.1 OPENING OR CLOSING A JUMPER

When modifying jumpers the board should be placed on a flat surface with the component side up. Make sure that the right jumper is to be modified (refer to Figure 1.1 and the silkscreen on the board). Take care not to let any solder splatters or metal flakes get on the board.

A closed jumper will have an electrical connection between the ends of the jumper (this may be a wire or a piece of foil on the board). An open jumper will have no electrical connection between the ends of the jumper (no wire or foil on the board).

The jumper may already be in the state desired and no modifying is needed.

To open a jumper is to remove the electrical connection, if a wire, then remove the wire, else if a foil then cut the foil. When cutting the foil make sure that it is the jumper foil that is going between the two ends of the jumper (jumper foils are on the component side only). To close a jumper is to make an electrical connection, to do this use a soldering iron and solder a wire between the two ends of the jumper (put the wire on the component side). The wire should be long enough to go between the jumper holes but not too long.

10.0 ZETACO DISK SECTOR FORMAT

The standard ZETACO sector format is shown below. Upon receiving a Write Format Command, the controller records the required gaps, ID Header and Data Field fill word onto each sector of the specified track. The ID Header is then only read to provide greater positive indication of the cylinder, head and sector address specified by a Read or Write Data Command.

	GAP 1	ID HEADER	GAP 2	SYNC	DATA	ECC	GAP 3
Bytes:	27**	7	17	1	*	4	11 **

Gap 1 - 27 bytes of zero (min.) for disk tolerance and PLO Sync

ID Header - Sync (1 byte)
Cylinder Address (2 bytes)
Head and Logical Sector Address (2 bytes)
ID Header CRC (2 bytes)

Gap 2 - 17 bytes of zero (min.) for write splice and PLO Sync

Sync - 1 byte for Data Field Synchronization

Data - Data Field: length may vary and is a function of the Drive Type Bank selected for the particular drive unit (see Addendum 1) the standard length is 256 bytes***

ECC - 4 bytes Data Field Error Correction Code

Gap 3 - 11 bytes of zero (min.) for end-of-sector tolerance

**NOTE: The two gaps may vary as a function of the drive.

***NOTE: With the Alternate Track Mapping option, the sync is fixed at 019 Hex and the Data Field is fixed at 256 bytes.

11.0 DISK MEDIA CONFIGURATION

This Section contains a basic description of disk addressing techniques used by the 990 SMD+. Because the 990 SMD+ offers control of drives of different capacities and physical characteristics, the number of cylinders, heads, sectors per track and interleave factor varies from drive to drive.

11.1 DISK ADDRESSING

The 990 SMD+ can control up to four logical disk units. Each unit contains one or more platters, and a head carriage assembly which positions the read/write heads over the data surfaces of the platters. The cylinder address is used in positioning the heads over the disk surface. The combination of a cylinder and head address specifies a particular track address of a surface.

Once the controller has directed the drive to a particular track, it locates the specified sector by reading and comparing the sector ID Headers. Once the cylinder, head and sector addresses are correctly verified, the controller may read or write the data field of the sector.

Using direct addressing, the 990 SMD+ may control up to 2048 cylinders and 32 heads (tracks per cylinder) per logical drive unit, and up to 128 sectors per track.

11.2 INTERLEAVING AND HEAD SKEWING

The 990 SMD+ uses sector interleaving to allow the controller sufficient time to finish sector operations and set-up for transfer of the next sequential sector. When the disk is formatted, the sector number written in the ID Header of each sector is not the true physical sector, but rather a number calculated by the controller based on the interleave factor for the particulr drive. The interleave factor is the number of physical sectors from one logical sector to the next sequential logical sector of a track.

Head skewing is used to allow the controller sufficient time after completing an operation on the last logical sector of a track to select the next head before logical sector zero passes under the head. The head skew is the number of physical sectors a surface's logical sectors are shifted forward with respect to those of the previous surface. The head skew required may vary from drive to drive due to head switching characteristics.

12.0 TROUBLE-SHOOTING PROCEDURES

When a problem occurs as a result of either equipment malfunction or installation configuration, diagnostics and visual inspection should be used to help locate the problem.

First, the ZETACO Reliability program and associated commands should be run on the controller to get specific information on the nature of the problem. Using the results should then simplify locating the problem. To use the RELI program, see Section 7.0.

If the ZETACO RELI is not available, examination of DX10 error codes and system log information for more specific results can also be useful.

If running diagnostics and consulting the following checklists cannot identify the problem, or the controller board appears to be malfunctioning, refer to the section "Customer Service" at the front of this manual for further assistance.

12.1 CONTROLLER CHECK

1. Does the controller pass Self-Test? Refer to Section 5.0 to determine if the controller board has an internal malfunction.

2. Check controller to drive cabling; see Section 3.6. Check for frayed or broken wires at cable plugs. Make sure "B" cables are in their proper headers on controller.

3. With power OFF, remove the controller and re-check all switches; see Section 3.3. Does the TILINE address selected match the operating system configuration?

12.2 DISK DRIVE CHECK

1. Is the shipping carriage lock on the drive, if any, in the unlocked position?

2. Refer to the drive documentation to verify switch settings. Does the manual clearly define switch position polarity regarding the table symbols? (1 = ON or OFF, etc.)

3. Is the drive set for the proper unit address?

4. Is the drive set for the proper number of sectors per track? This value may be found in Addendum 1 of this manual.

5. With some drives, the calculated value to set the sector size switch does not come out even, or is off a count. This may cause shortened sectors, or long sectors and a short last sector, resulting in search errors on pre-formatted packs or excessive bad tracks on new disks. When configuring a drive for the first time it may be necessary to adjust this setting up or down single counts until the correct sector size is found.

6. Are the drive cables connected with Pin 1 to Pin 1 of the headers? If the drive is dual port are the cables connected to the correct port connectors? Check cables for frayed or broken wires at the plugs.

7. Are all drives grounded together and to the chassis via ground strapping? See Section 3.6.1.

12.3 CHASSIS CHECK

1. Is the controller in the proper slot? A chassis configuration sheet should be used in selecting a slot with the proper TILINE priority in relation to other high speed controllers in the system.

2. Does the interrupt level of the slot match the operating system configuration? Is the interrupt taken from the same chassis connector that the controller is configured for? See Section 3.3.2.

3. Verify that the controller is the only device using the selected TILINE address.

4. Check to see that the access grant jumper has been removed from the chassis for the controller's slot, and the jumpers for all unused slots of lower priority are in place.

CUSTOMER SUPPORT HOTLINE

ZETACO, Inc. provides a Customer Support Hotline (612-941-9480) to answer technical questions and to assist with installation and troubleshooting problems.

The Hotline is manned by a technical team from 8:00 a.m. to 5:00 p.m. (Central Time) Monday through Friday.

WARRANTY INFORMATION

All ZETACO controllers and couplers are warranted free from manufacturing and material defects when used in a normal and proper manner for a period of two years from date of shipment. Except for the express warranties, stated above, ZETACO disclaims all warranties including all implied warranties of merchantability and fitness. The stated express warranties are in lieu of all obligations of liabilities on the part of ZETACO for damages, including but not limited to, special, indirect or consequential damages arising out of or in connection with the use or performance of ZETACO's products.

PRODUCT RETURN AUTHORIZATION

When controller malfunction has been confirmed, the board can be returned to ZETACO for warranty repair or for time-and-material repair if the product has been damaged or is out of warranty. An RMA number is required before shipment and should be referenced on all packaging and correspondence.

Each product to be returned requires a separate RMA number. To insure fastest response, the information outlined in the Material Return Information form on the following page should be gathered before calling the ZETACO Hotline for the RMA number. Please include a completed copy of the Material Return Information form with the product.

To safeguard your materials during shipment, please use packaging that is adequate to protect it from damage. Mark the box "Delicate Instrument" and indicate the RMA number(s) on the shipping label.

(include with returning material)

MATERIAL RETURN INFORMATION

All possible effort to test a suspected malfunctioning controller should be made before returning the controller to ZETACO, Inc. for repair. This will: 1) Determine if in fact the board is defective (many boards returned for repair are not defective, causing the user unnecessary system down-time, paperwork, and handling while proper testing would indicate the board is working properly). 2) Increase the speed and accuracy of a product's repair which is often dependent upon a complete understanding of the user checkout test results, problem characteristics, and the user system configuration. Checkout results for the 990 SMD+ Controller should be obtained by performing the following tests.

FUNCTION	TEST	RESULT
SMD	Selftest	_____
	Reliability	_____

Other tests performed:

Please allow our service department to do the best job possible by answering the following questions thoroughly and returning this sheet with the malfunctioning board.

1. Does the problem appear to be intermittent or heat sensitive? (If yes, explain).

2. What operating system and revision are you running under?

3. Describe the system configuration (i.e. peripherals, I/O controllers, model of computer, etc.).

4. Has the controller been returned before? Same problem?

To be filled out by CUSTOMER:

Model #:_____
Serial #:_____
RMA #:_____

Returned by:_____
(Company Name)

ZETA

Please give us your comments.

Please use this form to send us your comments regarding this Technical Manual. Your input is greatly appreciated! Problems will be promptly addressed and action taken as necessary. If you wish a written reply, please furnish your name and mailing address. Thank you.

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